

Arwen Block Diagram

H310UA1

FLEX Computing




Project Name : ARWEN UA1		Title : BLOCK Diagram	
Size : Custom	Document Number : HPMH-40GAB4000-D000	Rev : D	
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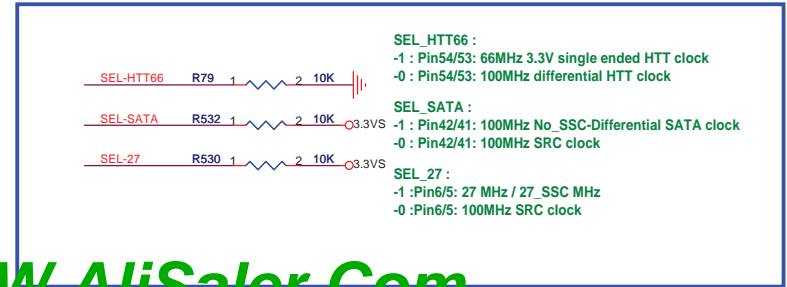
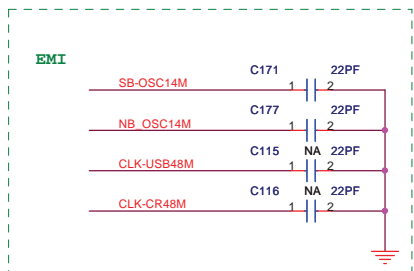
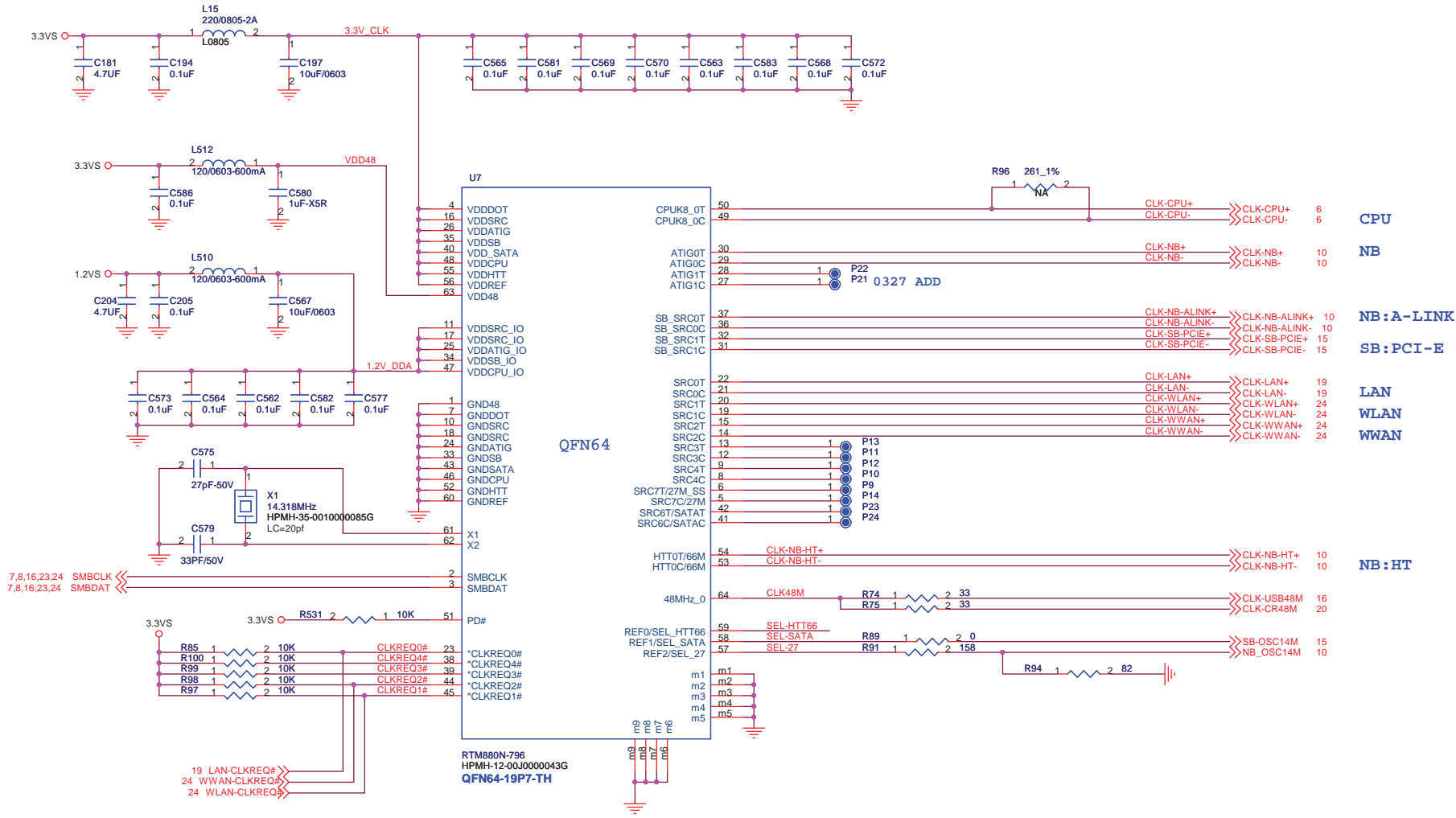
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
ACIN	~+19V	26	ADAPTER IN POWER		S0-S5
B+	+10~+19V	13,23,24,26,27,28,29,30,31,32,33	MAIN POWER		S0-S5
VBAT	+3.0V~+3.3V	15	RTC BATTERY		S0-S5
LDO5	+5V	22,29	LDO POWER	B+	S0-S5
LDO3	+3.3V	29	LDO POWER	B+	S0-S5
3.3VSTBY	+3.3V	15,16,17,22,25,26,29,31,33	STANDBY POWER	B+	S0-S5
3.3V-DUAL	+3.3V	15,16,17,18,25,31,33	EC CTRLD POWER	3.3VDUAL-ON#	BY EC CONTROL
1.2V-DUAL	+1.2V	18,31	3.3V-DUAL CTRLD POWER	3.3V-DUAL	BY EC CONTROL
5V	+5V	22,23,29,30,32,33,	SUS-C# CTRLD POWER	SUSC#	S0,S3
3.3V	+3.3V	13,33	SUS-C# CTRLD POWER	SUSC	S0,S3
1.8V	+1.8V	04,05,06,07,08,30,33	SUS-C# CTRLD POWER	SUSC#	S0,S3
0.9V	+0.9V	04,05,07,08,30	SUS-C# CTRLD POWER	SUSC#,SUSB#	S0,S3
5VS	+5V	06,13,14,17,18,21,22,23,25,27,28,31,32,33	SUS-B# CTRLD POWER	SUSB	S0
3.8VS	+3.8V	23,33	SUS-B# CTRLD POWER	SUSB#	S0
3.3VS	+3.3V	03,06,07,08,10,11,12,13,14,16,17,18,20,21,22,23,24,25,27,28,29,31,32,33	SUS-B# CTRLD POWER	SUSB	S0
2.5VS	+2.5V	06,31	SUS-B# CTRLD POWER	SUSB#	S0
1.8VS	+1.8V	06,10,11,12,15,16,33	SUS-B# CTRLD POWER	SUSB	S0
1.5VS	+1.5V	11,12,16,24,28,31,32	SUS-B# CTRLD POWER	SUSB#	S0
1.2VS	+1.2V	04,06,11,15,17,18,32	SUS-B# CTRLD POWER	SUSB#	S0
1.1VS	+1.1V	09,10,11,12,31	SUS-B# CTRLD POWER	SUSB#	S0
CPU_CORE		04,27	CPU CORE POWER	SUSB#	S0
NB_CORE	+1.0V~+1.1V	11,18,32	NORTH BRIDGE CORE POWER	1.1VS-PG	S0
BATA+	+10V~+17V	26	MAIN BATTERY		S0-S5

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	
 AGND	19	
 LAN-GND	21	

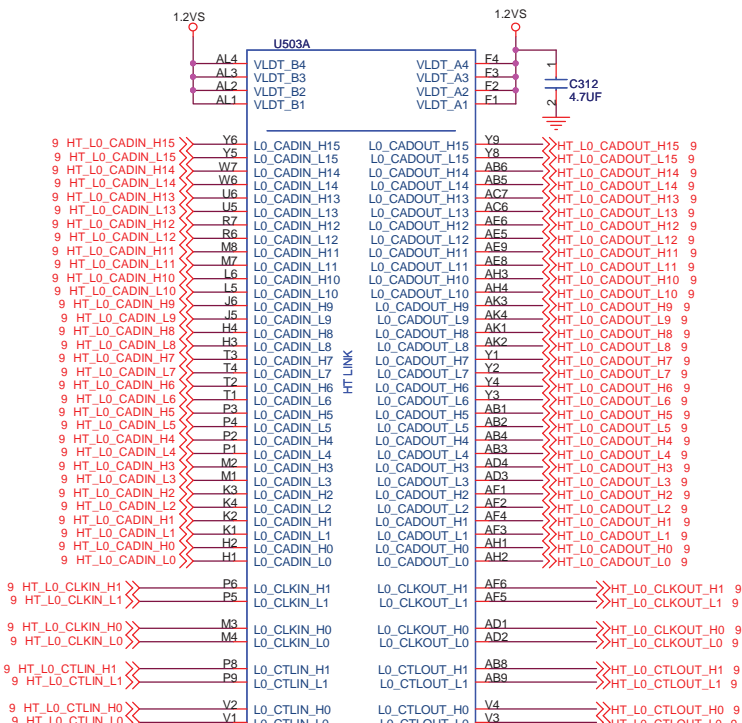
<b>FLEX Computing</b>		
Project Name : ARWEN UA1		Title : Power Diagram
Size : Custom	Document Number : HPMH-40GAB4000-D000	Rev : D
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# CLOCK GENERATOR

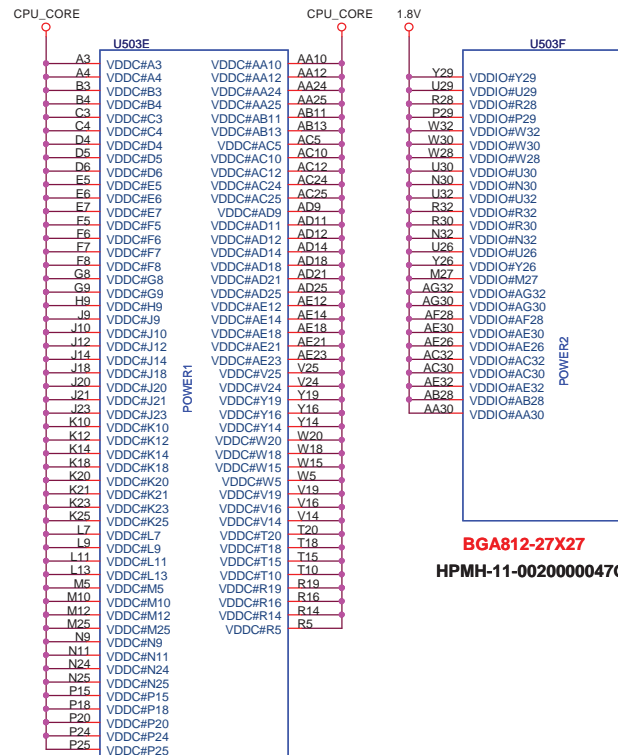


<b>FLEX Computing</b>		
Project Name : ARWEN UA1		Title : CLOCK GENERATOR
Size : A3	Document Number : HPMH-40GAB4000-D000	Rev : D
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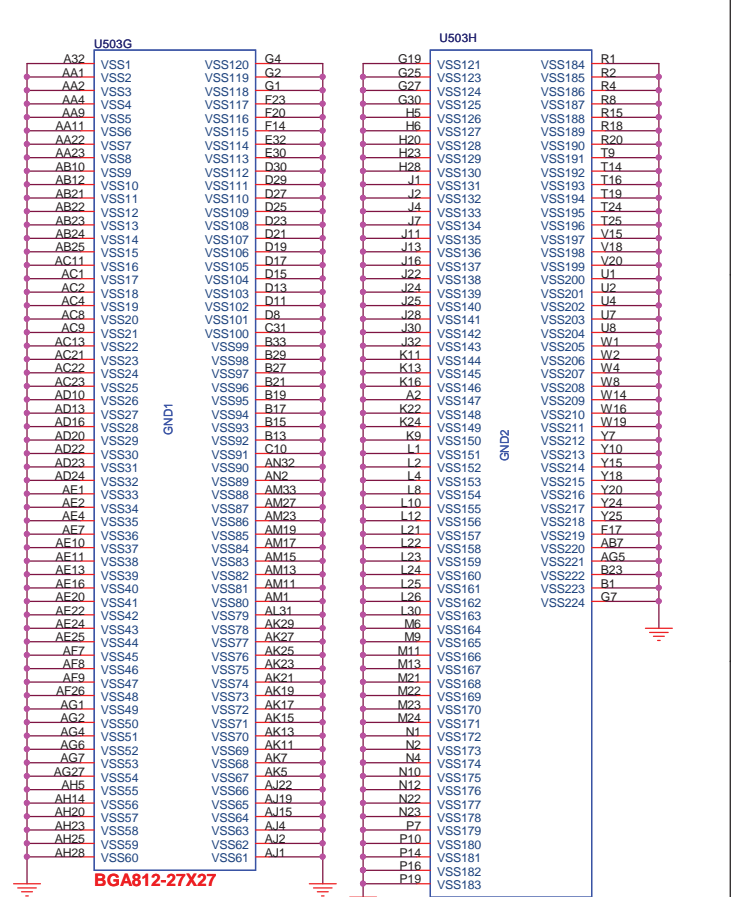
VLDT Trace at least 200 mils wide



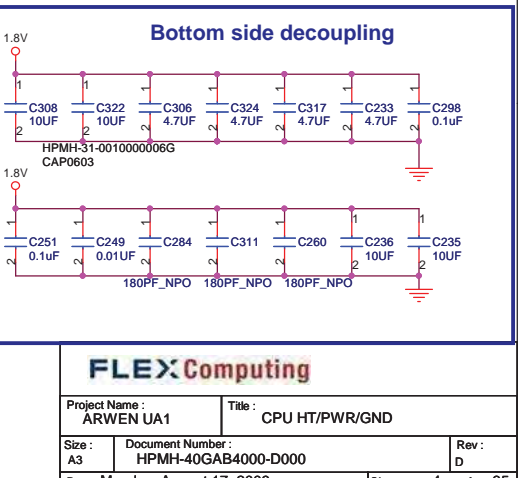
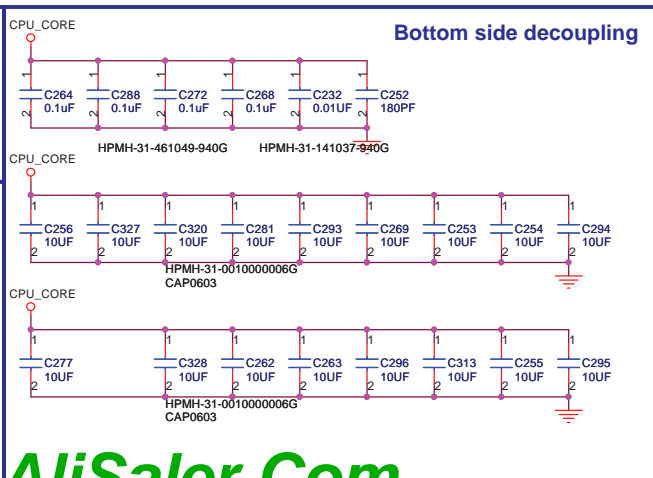
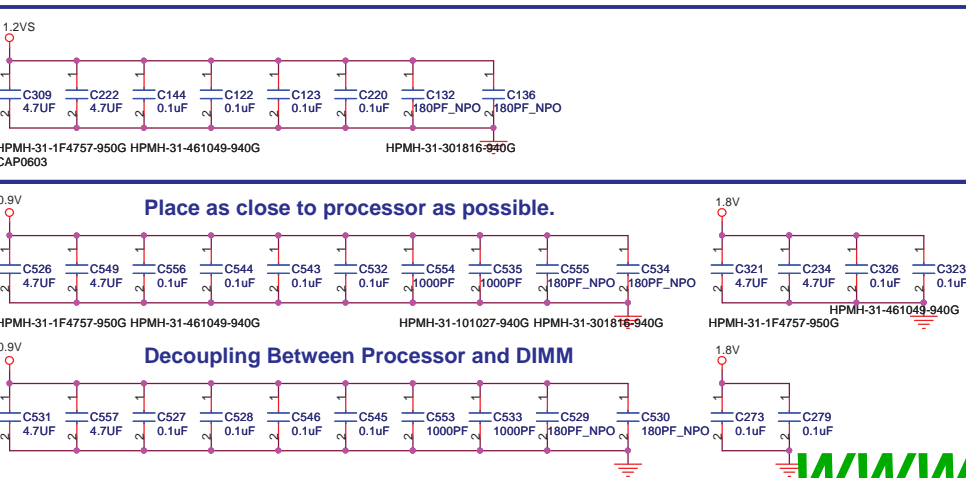
BGA812-27X27  
HPMH-11-0020000047G



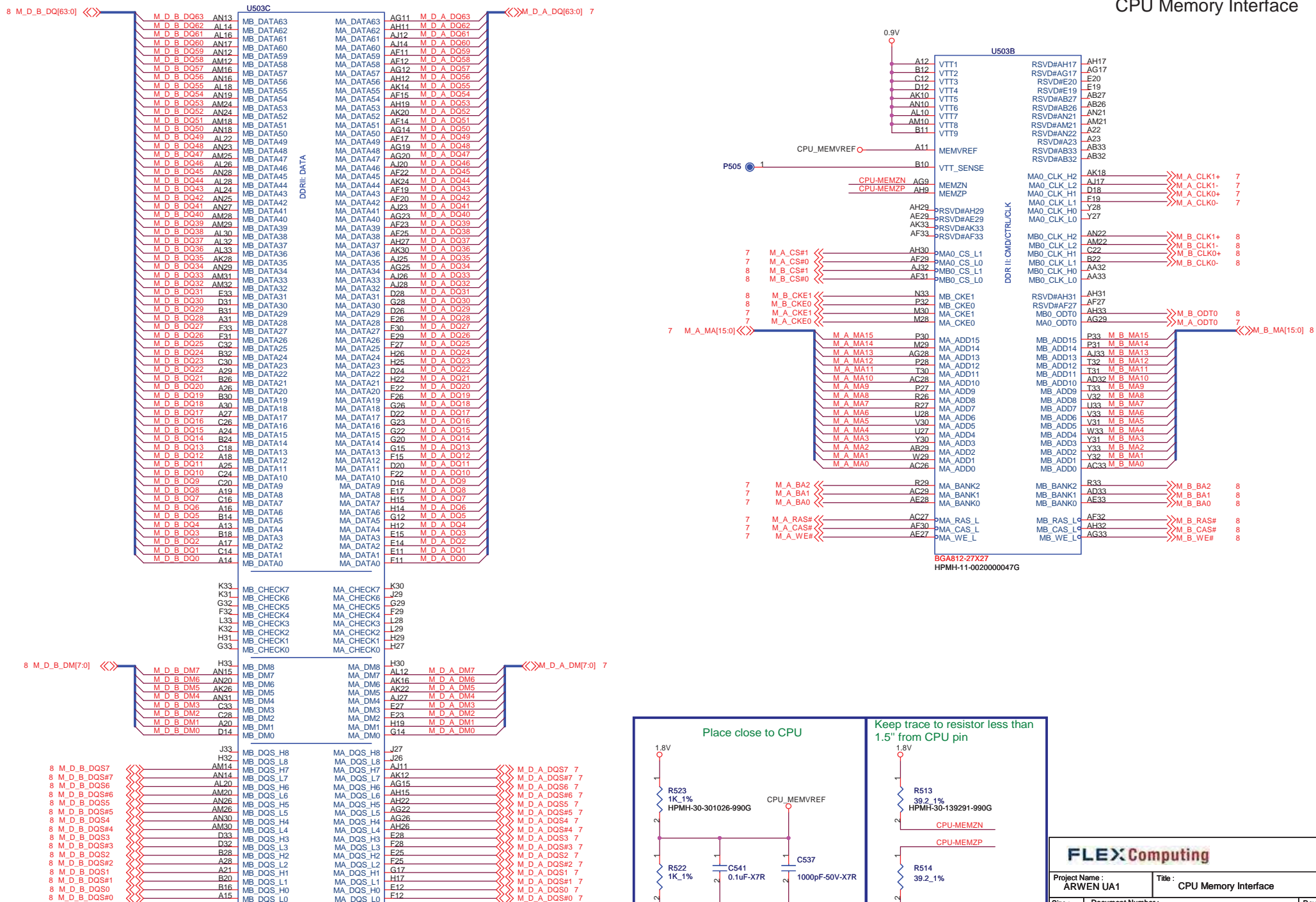
BGA812-27X27  
HPMH-11-0020000047G



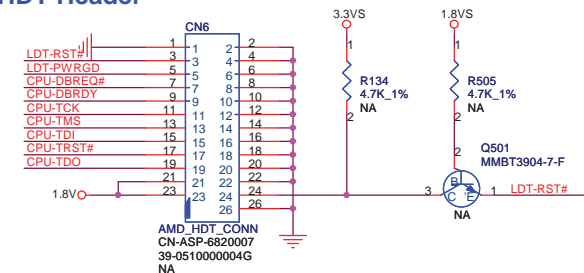
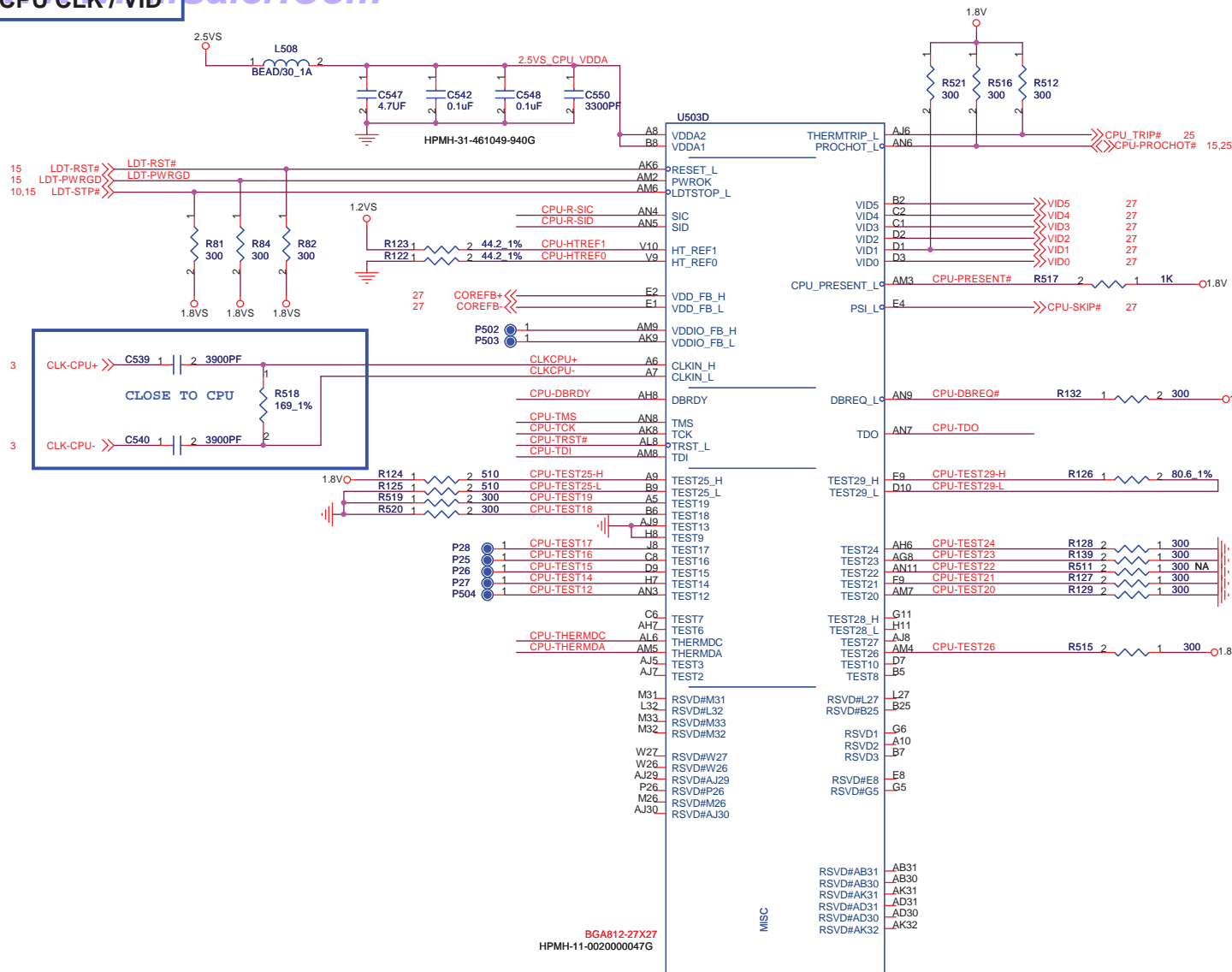
BGA812-27X27  
HPMH-11-0020000047G



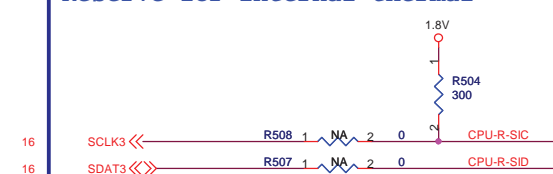
## CPU Memory Interface







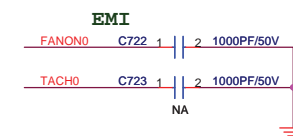
Reserve for internal thermal



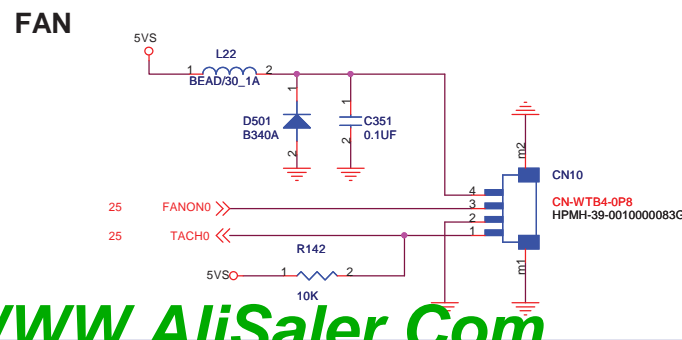
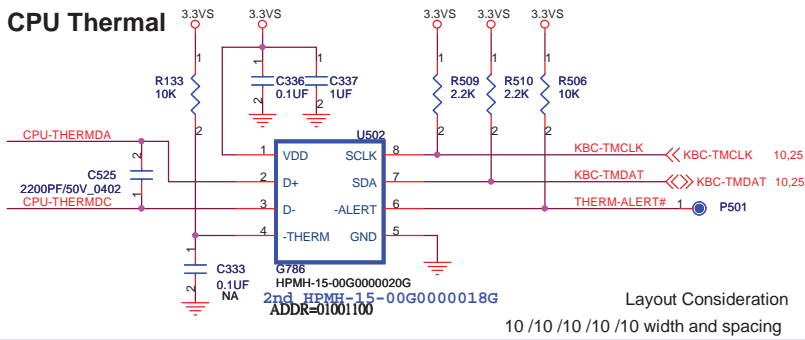
Delete LDT-STP# delay circuit for RS780 DA  
ER RS690B3

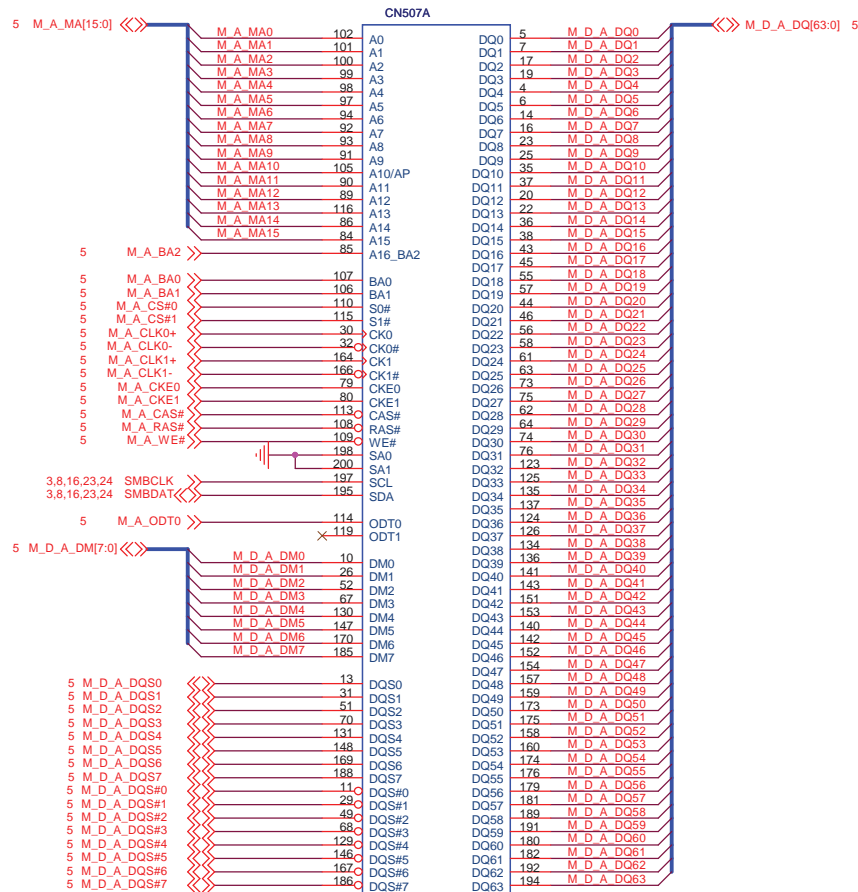
**Layout (1) :Keep trace to resistor less than 600 mils from CPU pin and trace to AC caps less than 1250 mils**

**Layout (2) :Route VDDA trace approx. 50 mils wide (use 2x25 mil traces to exit ball field) and 500 mils long.**

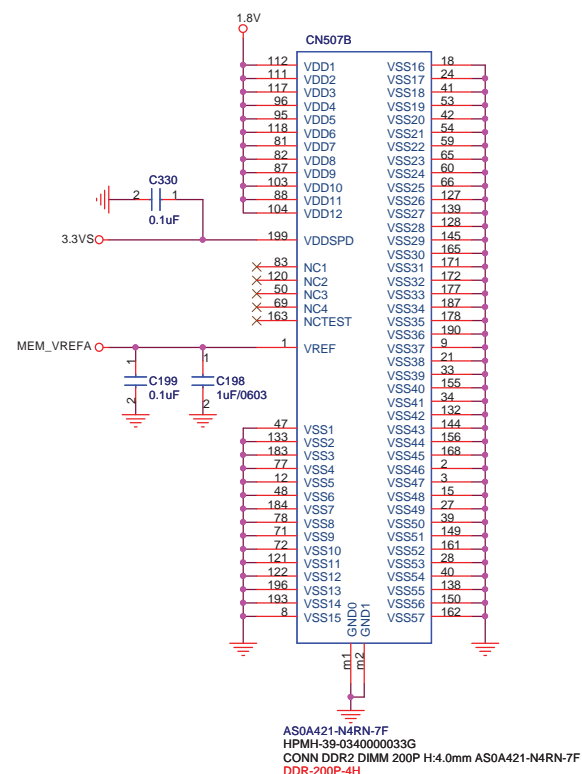


Project Name : ARWEN UA1		Title : CPU Control & Debug	
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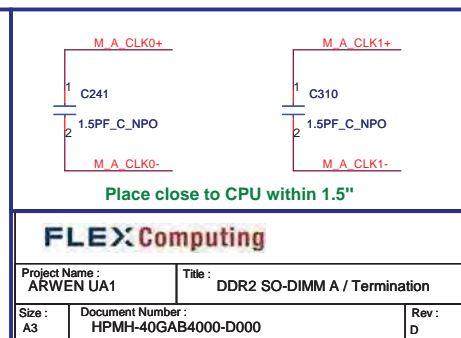
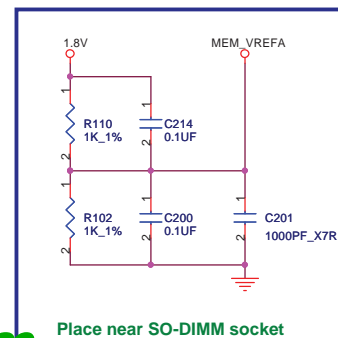
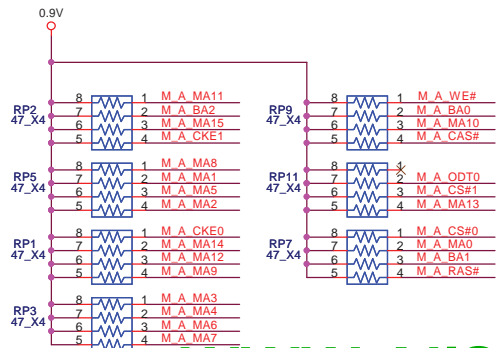
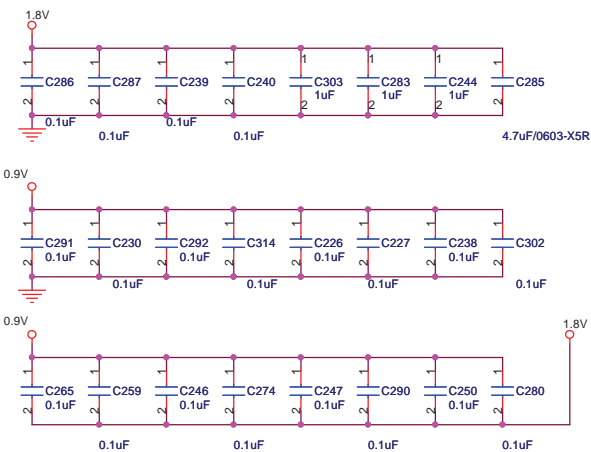


AS0A421-N4RN-7F  
HPMH-39-0340000033G  
CONN DDR2 200P H:4.0mm AS0A421-N4RN-7F  
DDR-200P-4H



AS0A421-N4RN-7F  
HPMH-39-0340000033G  
CONN DDR2 DIMM 200P H:4.0mm AS0A421-N4RN-7F  
DDR-200P-4H

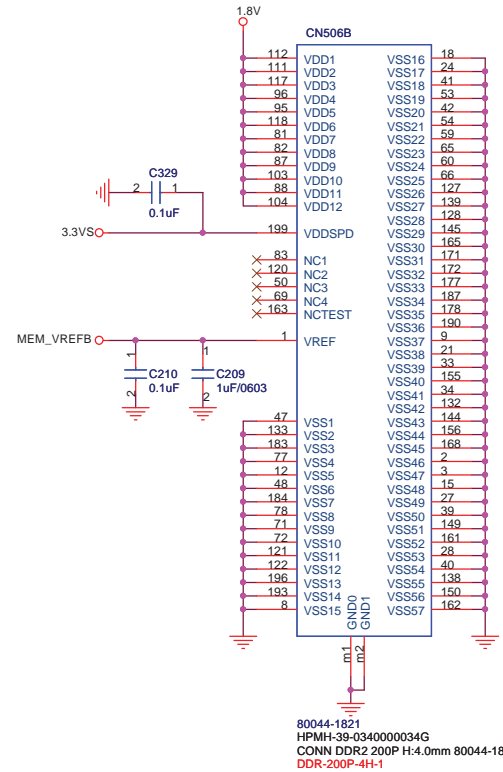
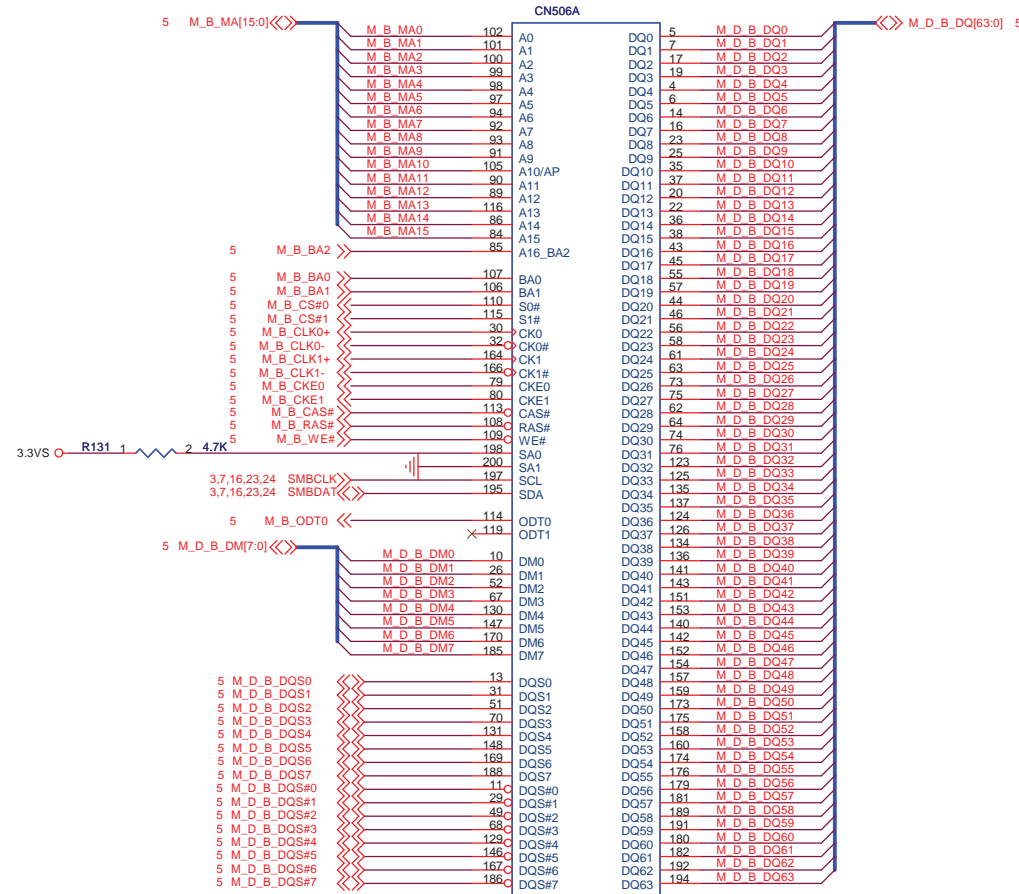
Layout :  
Place these Caps near So-DimmA



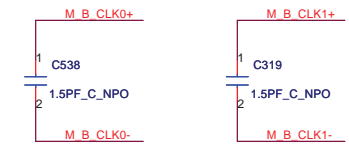
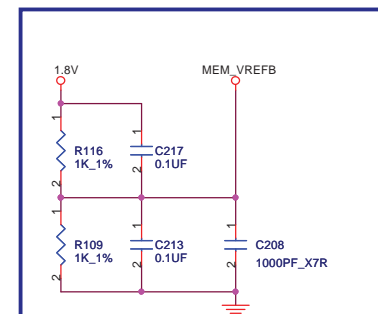
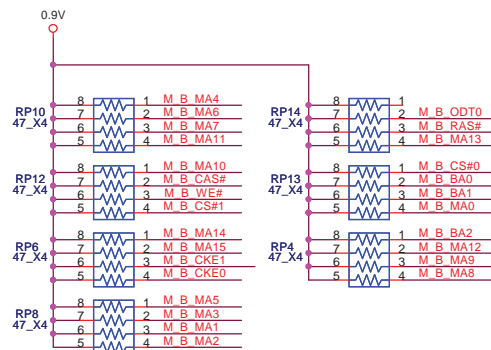
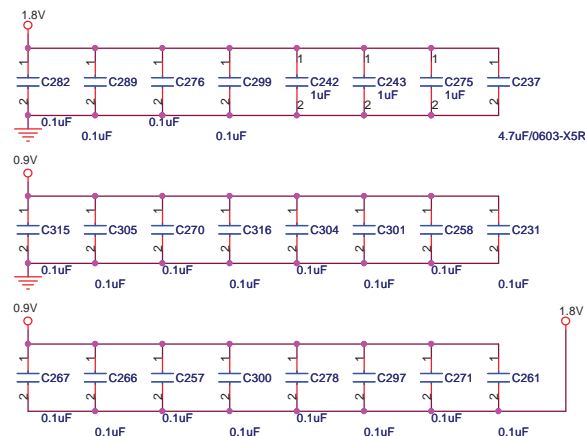
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Project Name : ARWEN UA1		Title : DDR2 SO-DIMM A / Termination	
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DDR2 Termination  
DDR2 SO-DIMMB



Layout :  
Place these Caps near So-DimmA



**Place close to CPU within 1.5"**

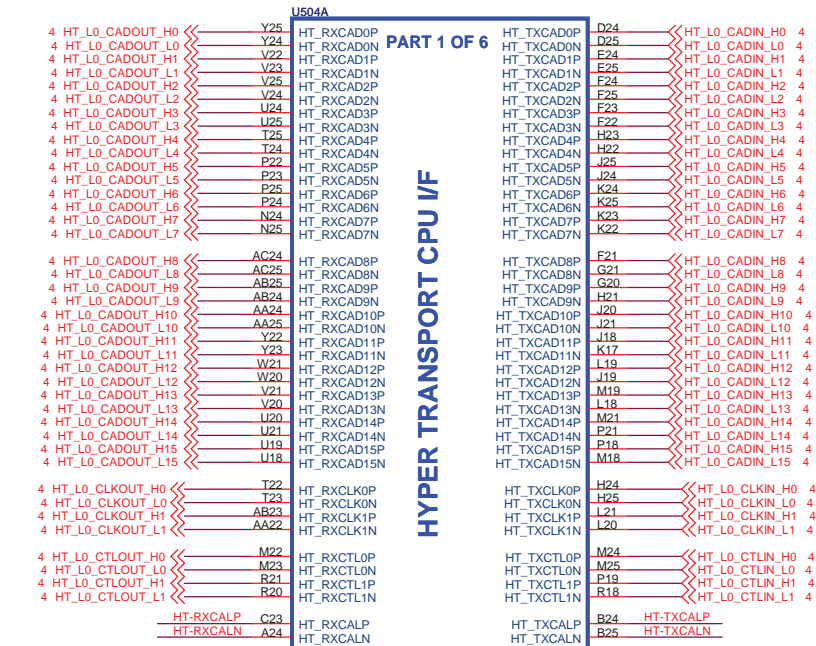
**FLEX** Computing

Project Name : ARWEN UA1	Title : DDR2 SO-DIMM B / Termination
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Size : A3	Document Number : HPMH-40GAR4000-D000	Rev : D
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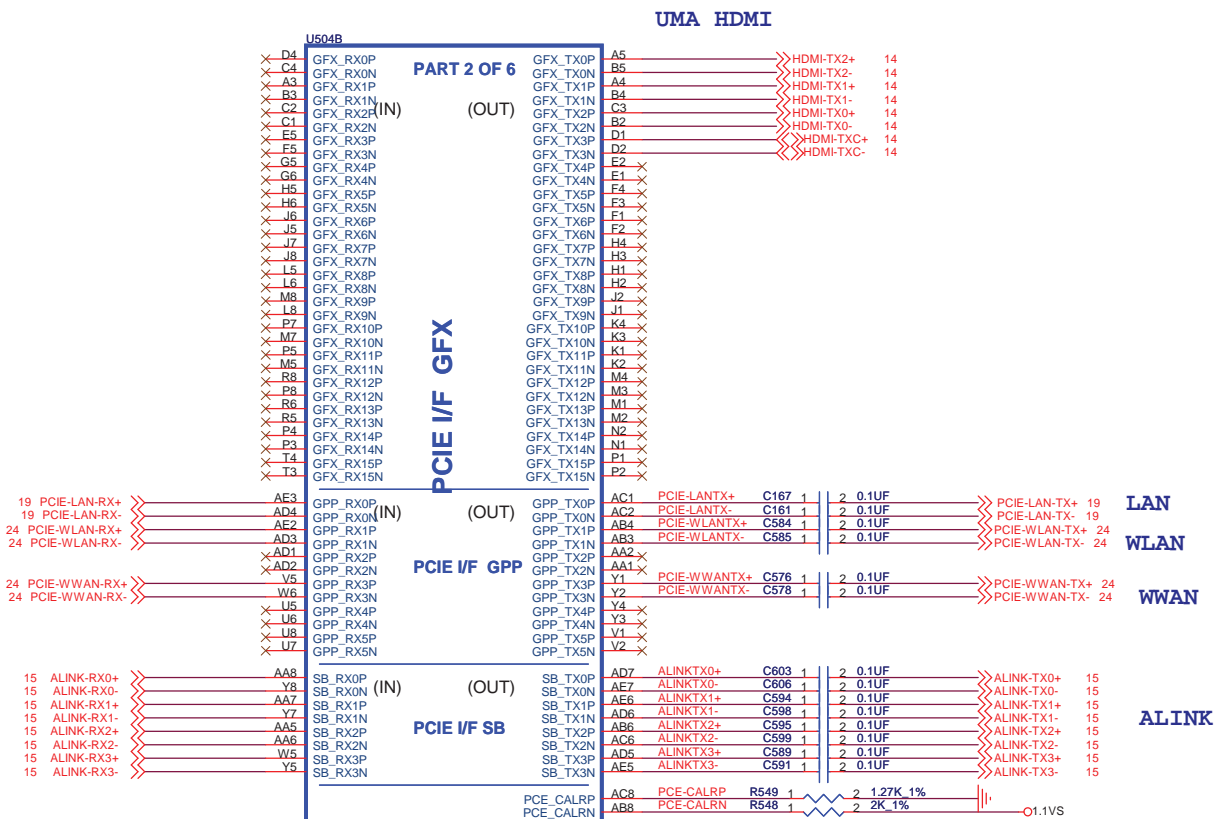
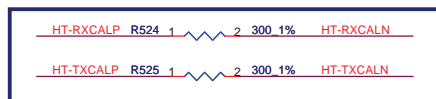
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RS780MN  
HPMH-10-0010000050G  
FCBGA528-RS780M

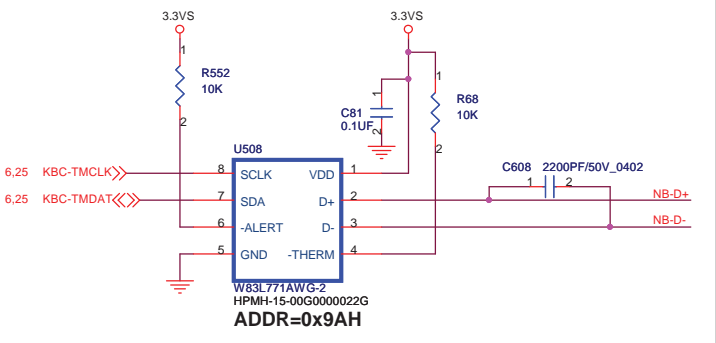
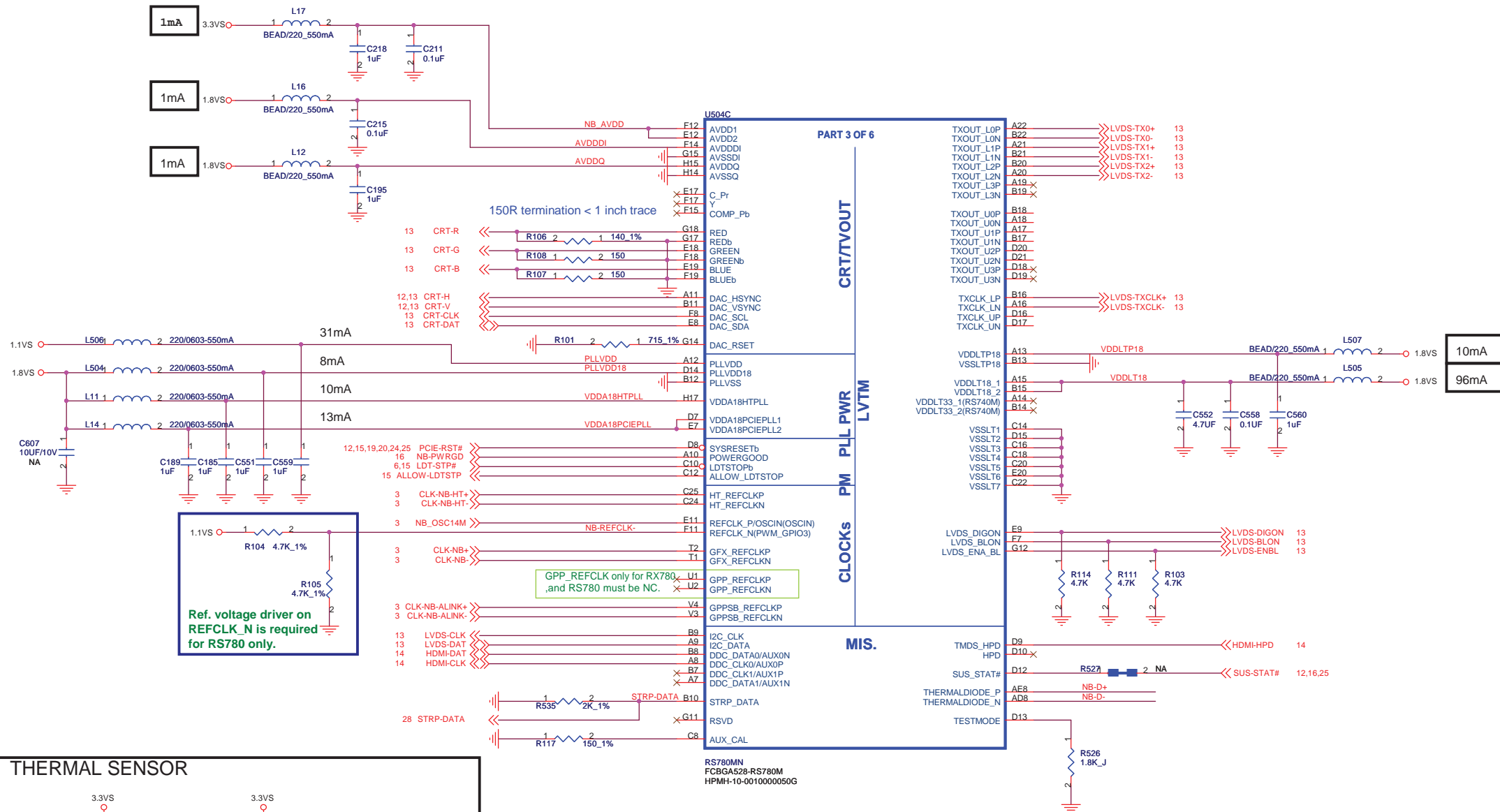
301 ohm to 300 ohm

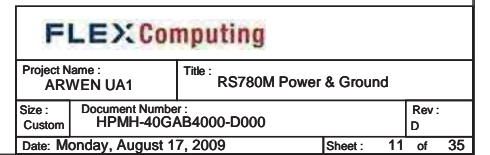


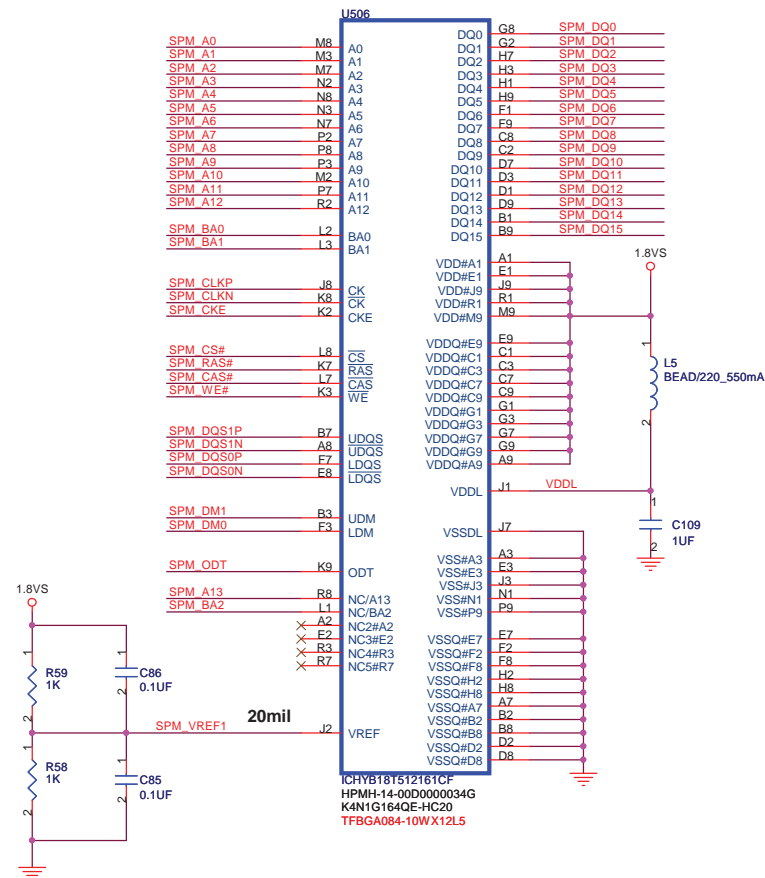
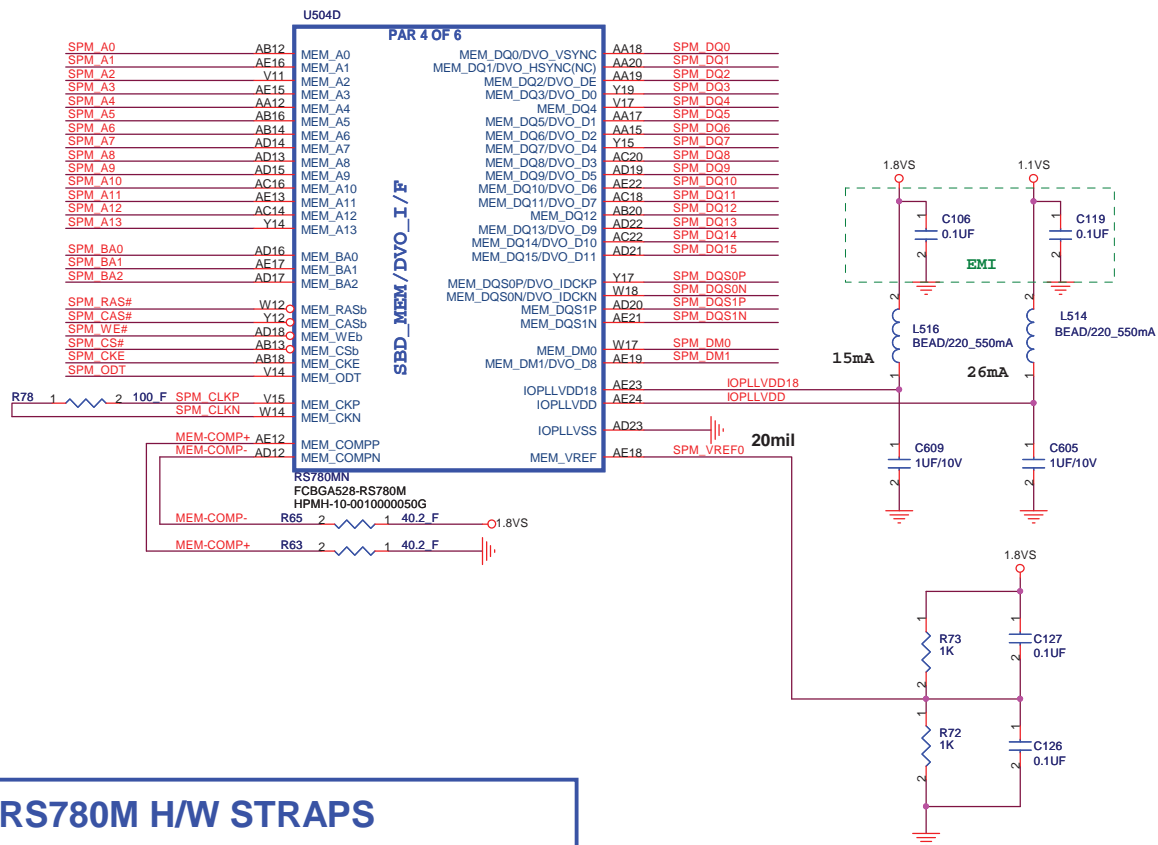
RS780MN  
HPMH-10-0010000050G  
FCBGA528-RS780M

**FLEX Computing**

Project Name : ARWEN UA1		Title : RS780M HT/PCIE/HDMI Interface	
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## RS780M H/W STRAPS

### STRAP\_DEBUG\_BUS\_GPIO\_ENABLE

Enables the Test Debug Bus using GPIO.  
DAC\_VSYNC (RS780.Pin B11)  
1 : Disable (RS780) ( default )  
0 : Enable (RS780)



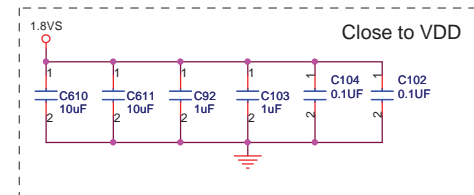
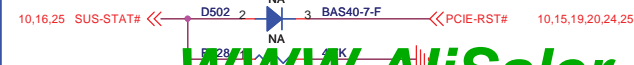
### RS780: Enable Side Port Memory

Selects if Memory SIDE PORT is available or not  
DAC\_HSYNC (RS780.Pin A11)  
1 : Disable (default)  
0 : Enable  
Register Readback of strap:  
NB\_CLKCFG:CLK\_TOP\_SPARE\_D[1]



### DFT\_GPIO1: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM  
SUS\_STAT# (RS780.Pin D12)  
-1\*: Bypass the loading of EEPROM straps and use Hardware Default Values  
-0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected



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Project Name : ARWEN UA1		Title : RS780M SBD / STRAPS	
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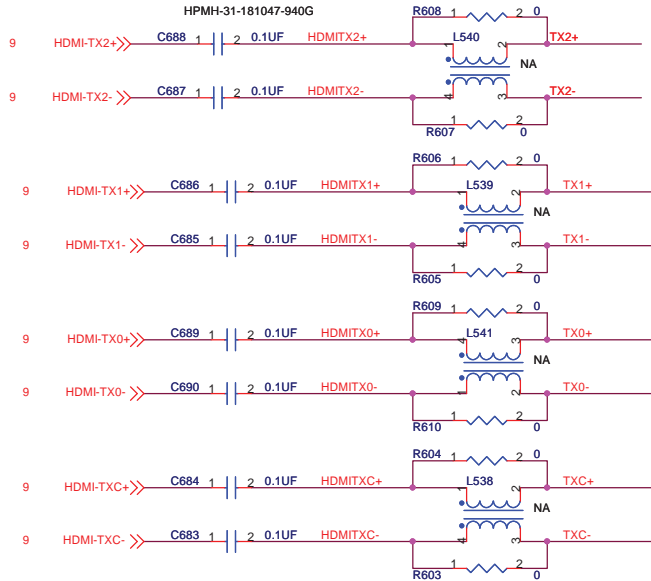
**WWW.AliSaler.Com**



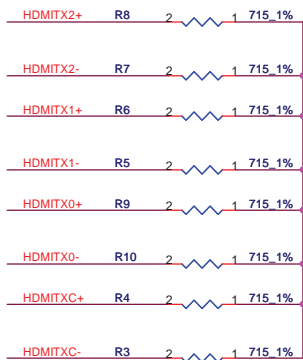
CLOSE CN5031

HPMH-32-4000000104G

HPMH-31-181047-940G



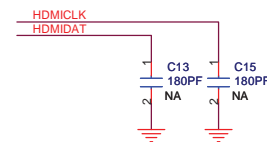
M92 SPEC SET 499 ohm



5VS

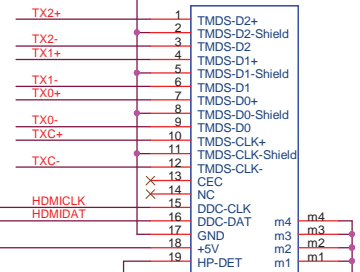
M1  
ME2N7002W

EMI



HDMI

CN515



CN-HDMI-19DIP-5H55  
HPMH-38-00F000008G

D6  
UDZ5V6B-7-F\_5.6V\_0.2W  
HPMH-20-000042-870G

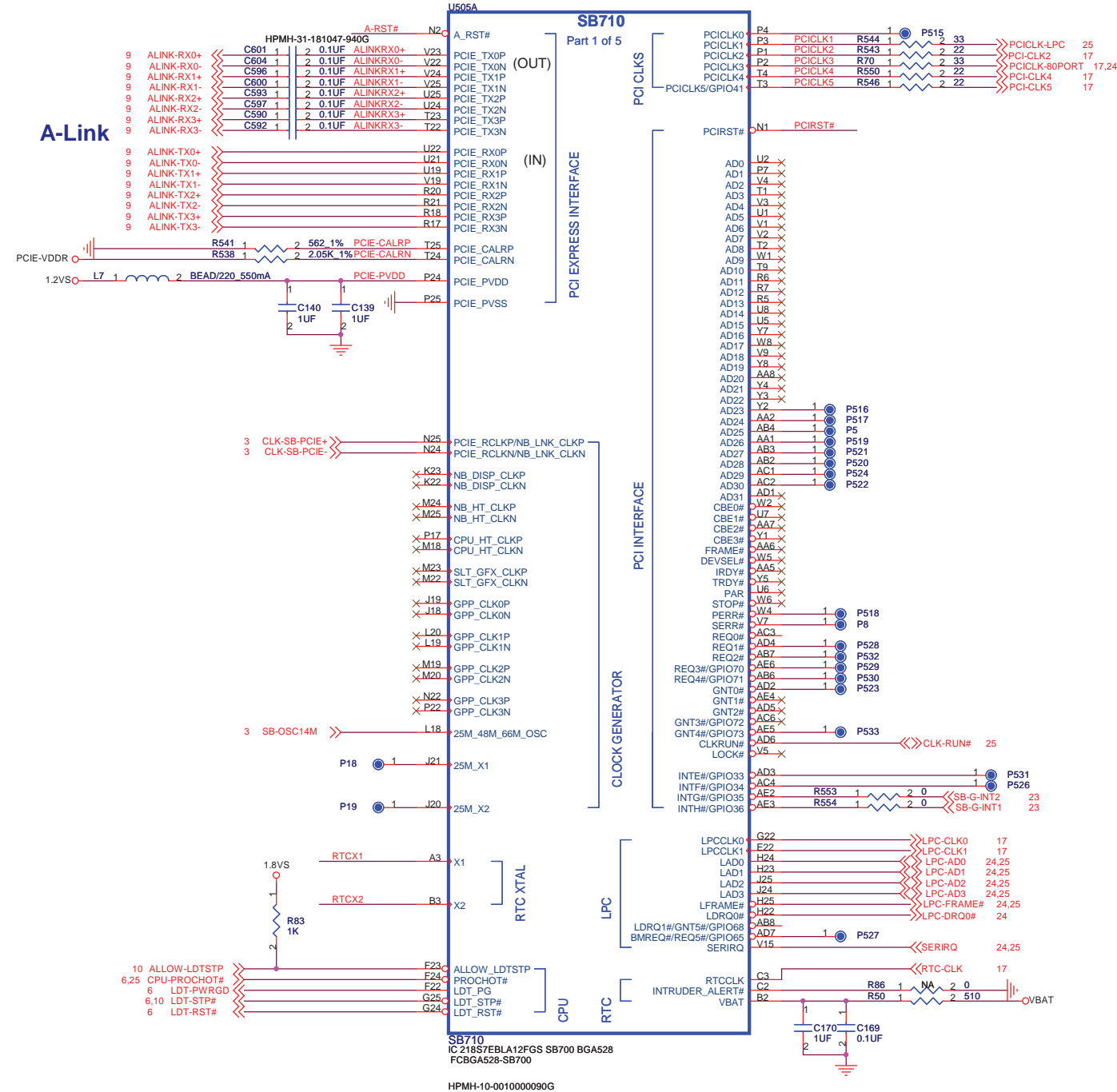
C17  
180PF  
EMI

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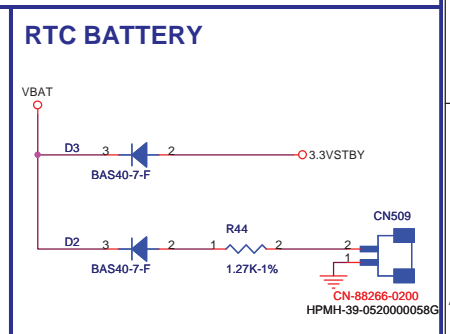
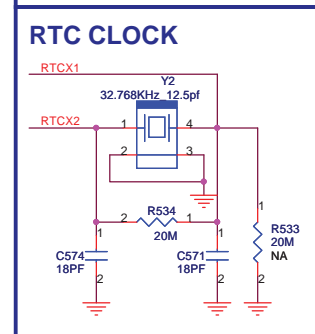
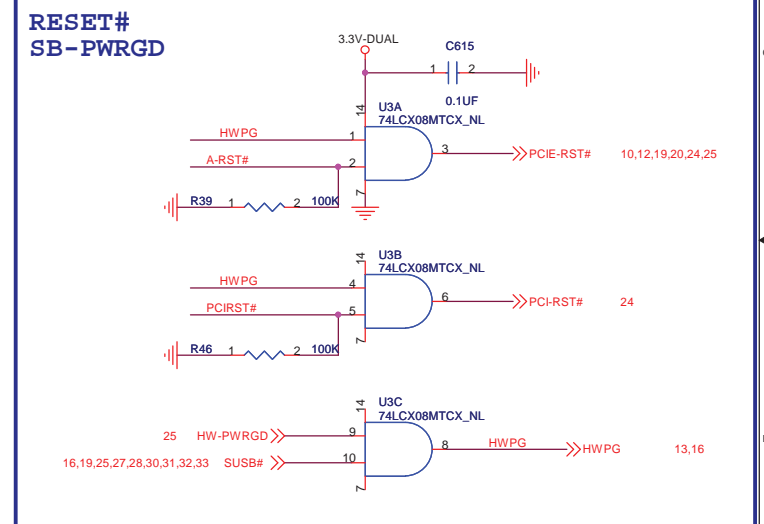
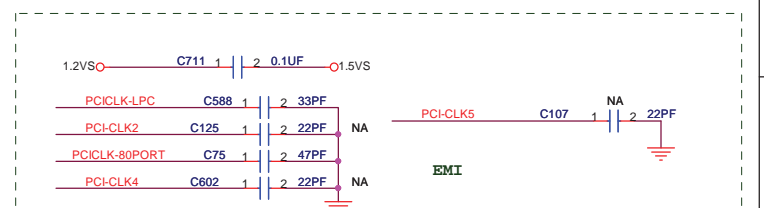
Project Name : ARWEN UA1 Title : HDMI Connector

Size : A3 Document Number : HPMH-40GAB4000-D000 Rev : D

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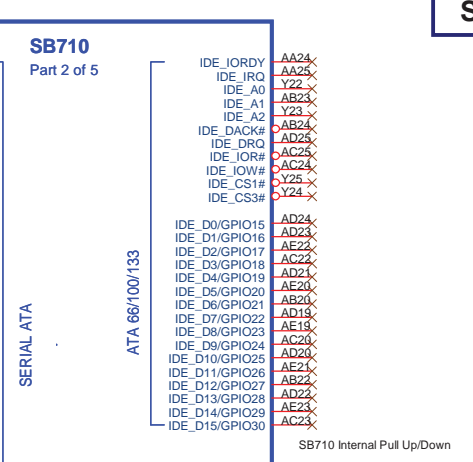
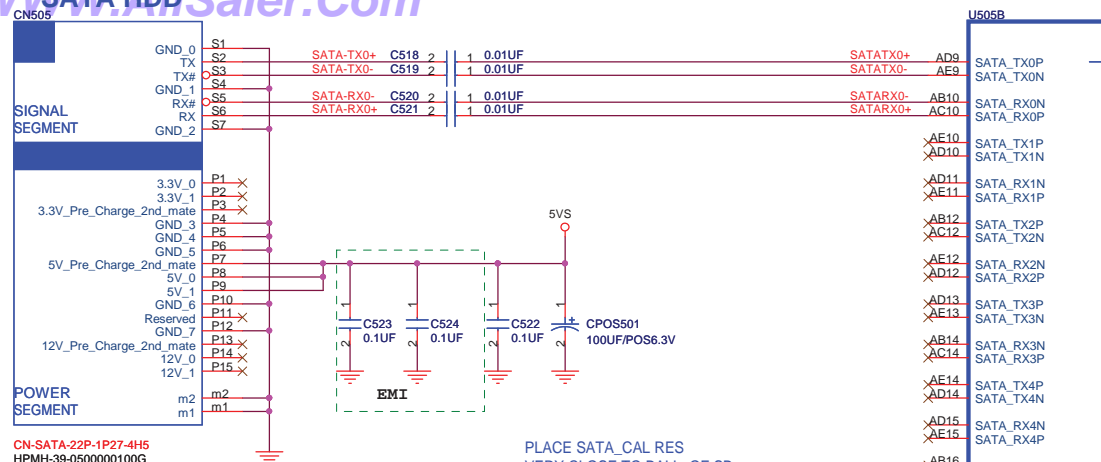
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



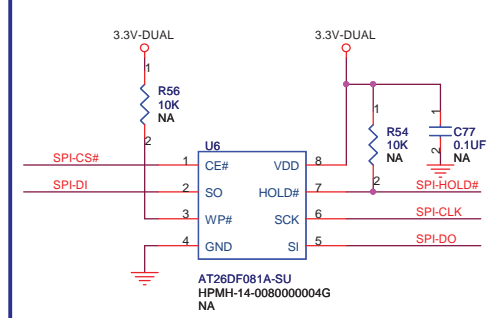
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Project Name : ARWEN UA1	Title : SB700 PCIE/PCI/CPU/LPC
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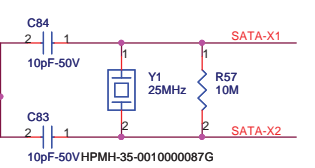




### Reserve 8M-bit SPI ROM



### SATA 25MHz

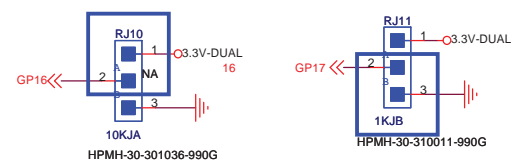


93 mA

6 mA

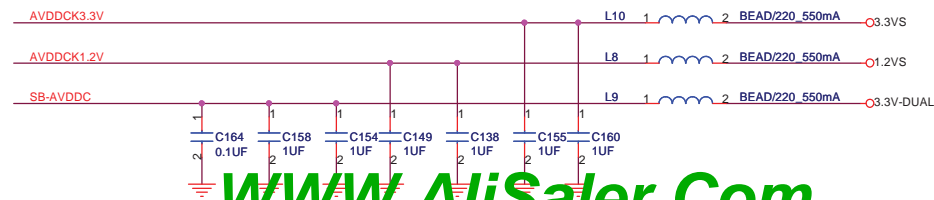
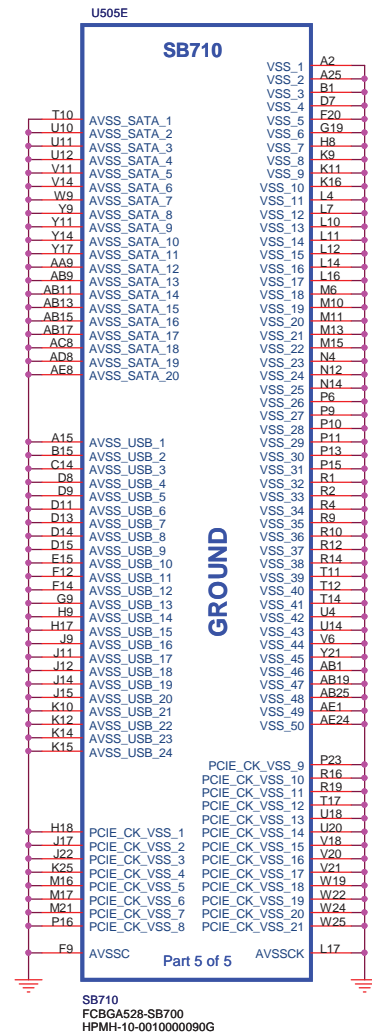
5 mA

### SB710 H/W STRAPS

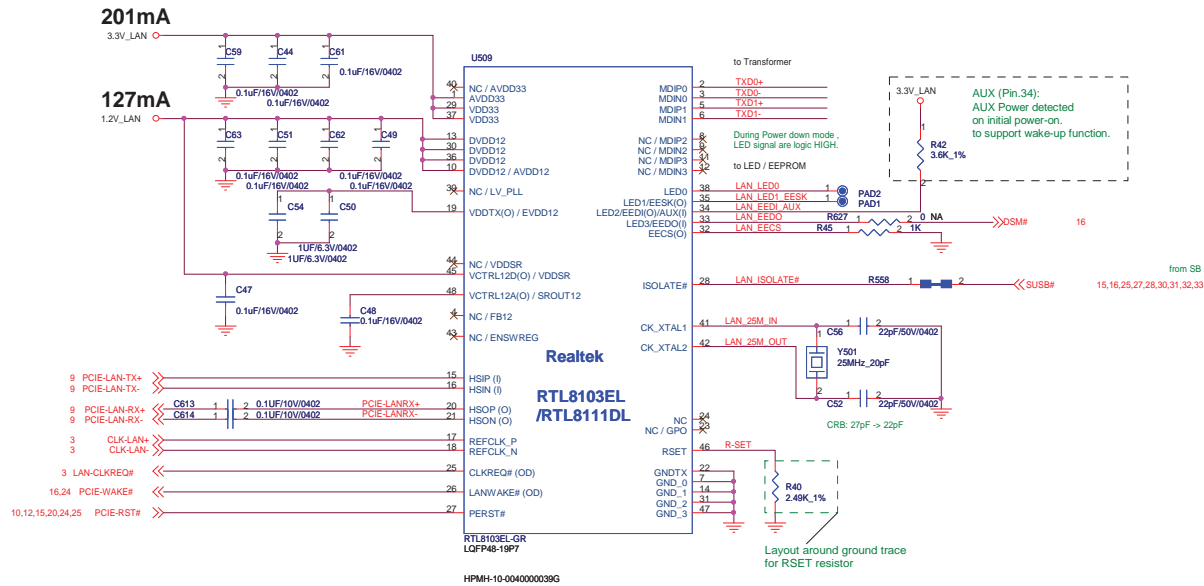


NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

	PCI-CLK2	PCI-CLK3	PCI-CLK4	PCI-CLK5	LPC-CLK0	LPC-CLK1	RTC-CLK	AZ-RST#	GP17	GP16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT (A11) IMC ENABLED (A12)	CLKGEN ENABLED	INTERNAL RTC DEFAULT	IMC ENABLED (A11) ENABLE PCI MEM BOOT (A12)	H,H = Reserved H,L = SPI ROM (Default)	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT (A11) IMC DISABLED (A12) DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC)	IMC DISABLED (A11) DISABLE PCI MEM BOOT	L,H = LPC ROM L,L = FWH ROM	







#### RTL8103E LED Configuration:

LED1-0	100	01	10	11
LED0	Tx/Rx	LINK	Tx	Tx
LED1	LINK100	LINK	LINK	LINK100
LED2	LINK10	LINK	LINK	LINK10
LED3	NA	NA	NA	NA

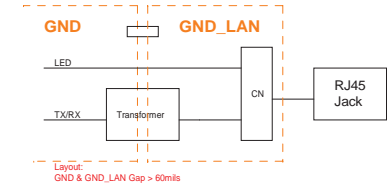
LED31-0's initial value comes from the 93C46  
If there is no 93C46, the default value is 00

#### H310 mini-spec\_v1.4

##### LAN LED:

- Amber : Activity (RX/TX)
- Green : Connectivity (Link)

#### Layout notes:



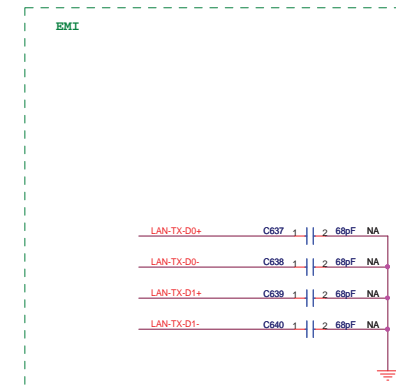
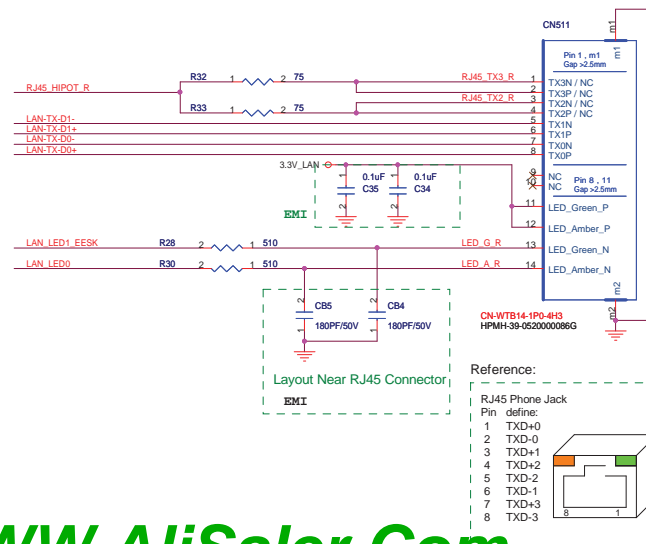
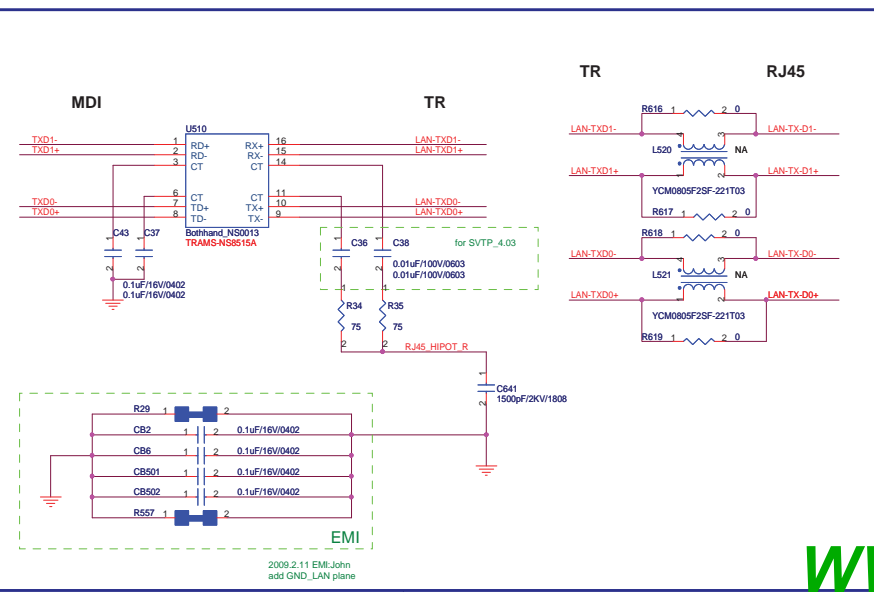
#### SVTP\_v4.03

##### 2.6 - Ethernet Checklist - Rev C.xls

- Ch.3.1.4.4  
Some older cheap RJ-45s only populate pins 1,2,3,6.  
10/100 requires the other 4 pins for grounding. Gigabit Ethernet requires all 8 pins for data signals.

- Ch.3.1.4.13  
Resistance from RJ-45 shell to any other chassis ground point (ohms) less than 1 ohm

- Ch.3.1.4.14 & Ch.3.1.4.15  
Protection against non-standard power-over-Ethernet (PoE) :  
Resistance between pins 1,3 (TXD0P, TXD1P) and pins 4,7 (TXD2P, TXD3P) of the RJ-45 greater than 58K ohms.

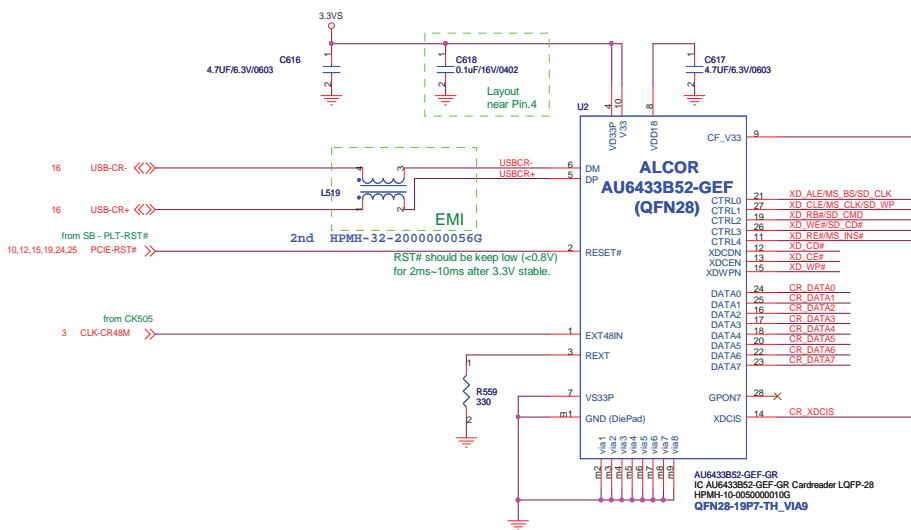


#### FLEX Computing

Project Name :	ARWEN UA1	Title :	RTL8103EL (LQFP48)
Size :	C	Document Number :	HPMH-40GAB4000-D000
Date :	Monday, August 17, 2009	Rev :	D
		Sheet :	19 of 35

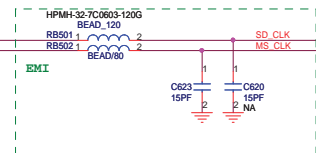
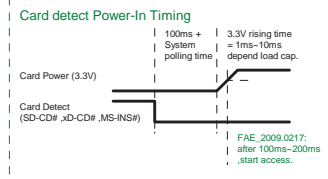
Alcor AU6433-GEF Card supported:

- SD v2.0 (SDHC)
- MMC v4.2
- MS v1.43
- MS-PRO v1.03
- MS PRO-HG v1.01
- xD v1.2



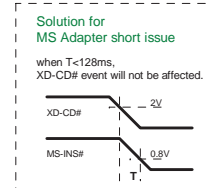
Card Power V33 = 3.3V ~ 2.8V  
Card Power OCP = 420mA

FAE\_2009.0217:  
CF\_V33 Internal P/D 1Kohm  
for power-off discharge

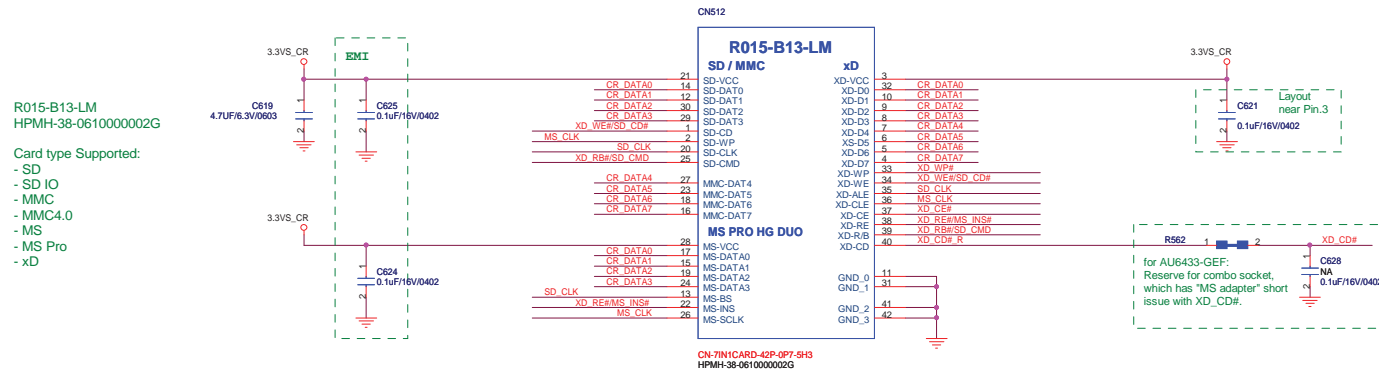


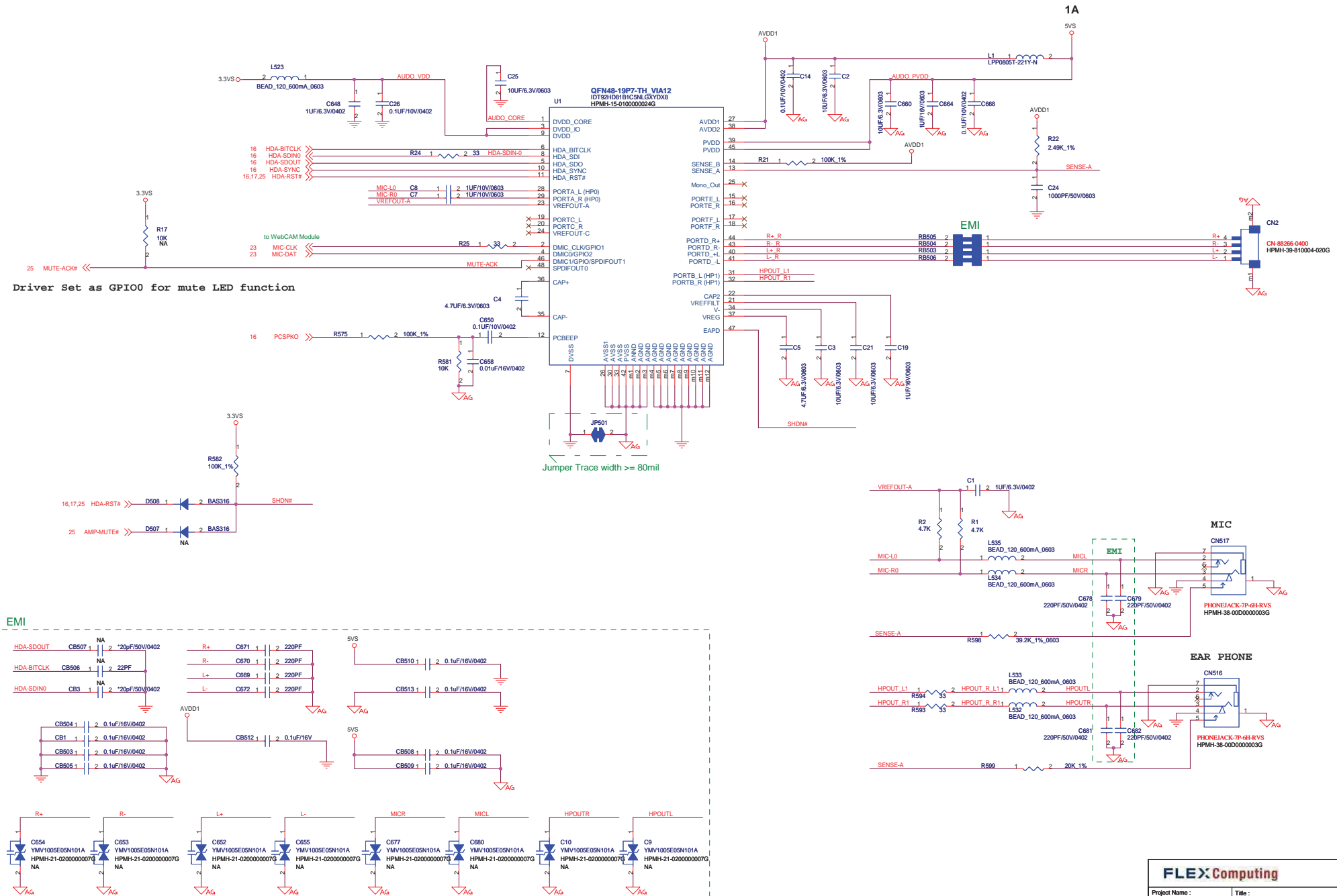
FAE\_2009.0117:  
Memory Stick Formatter for MS Logo  
- Enable

FAE\_2009.0117:  
SD write protect  
- Decided by SD-WP of SD Card



### Memory Card Socket



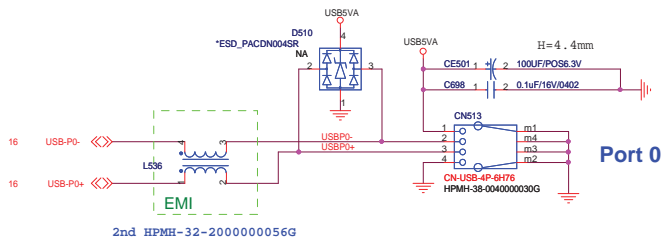


Driver Set as GPIO0 for mute LED function

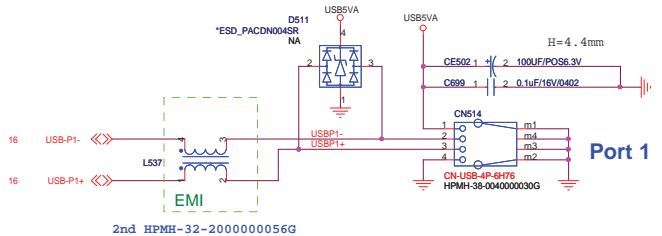
EMI

FLEX Computing

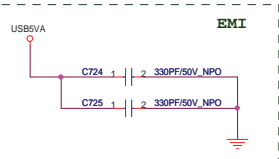
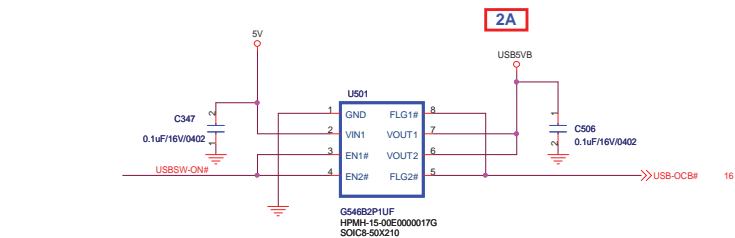
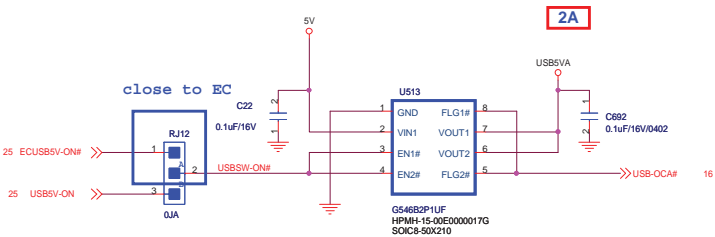
Project Name : ARWEN UA1		Title : HDA CODEC(92HD81)	
Size : C	Document Number : HPMH-40GAB4000-D000	Rev : D	
Date : Monday, August 17, 2009		Sheet : 21 of 35	



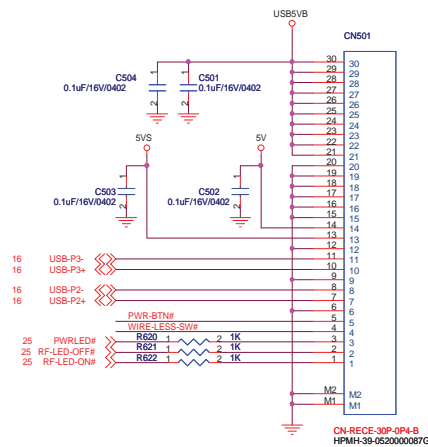
Port 0



Port 1

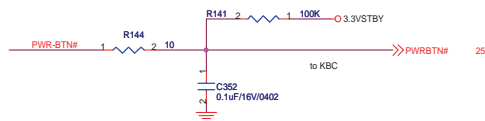


## USB DB CONN

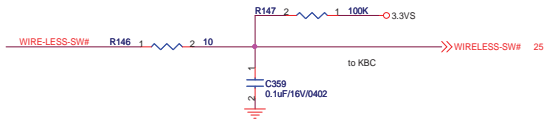


USB Power Connector needs >2A

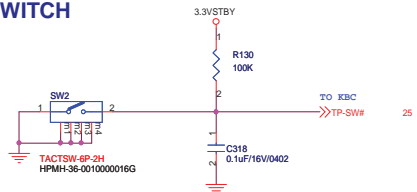
## Power ON/OFF Button



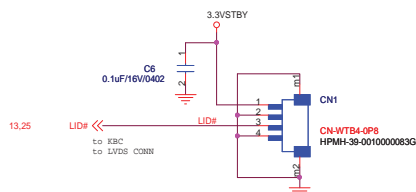
## Wireless ON/OFF Button



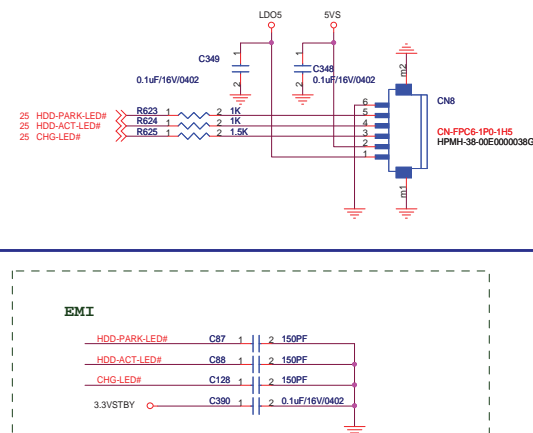
## TP LOCK SWITCH



## LID Switch



## LED DB CONN

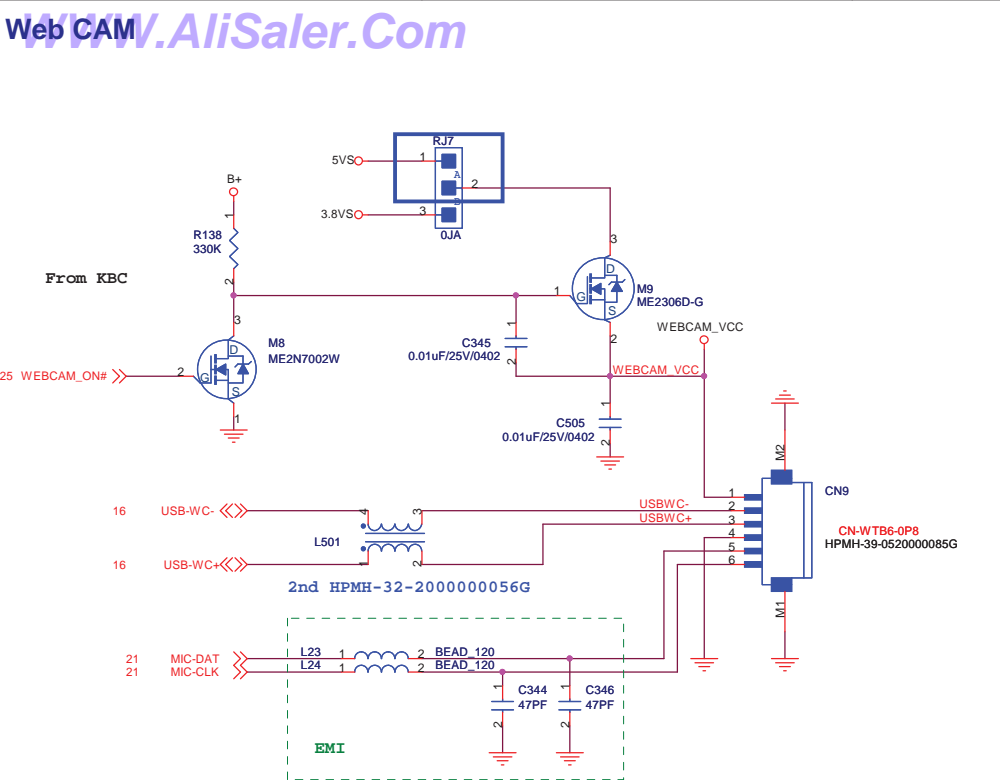


EMI

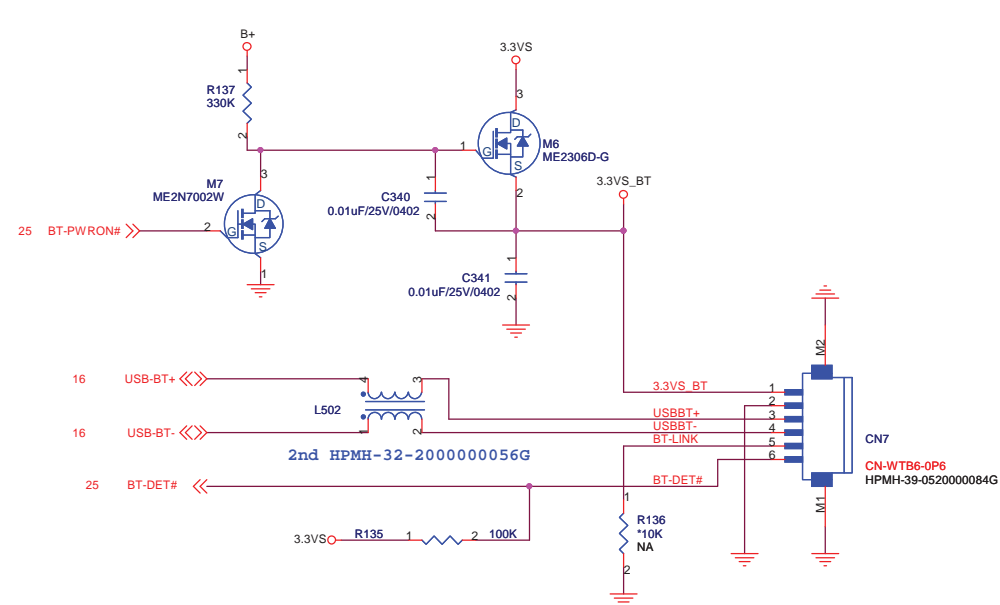


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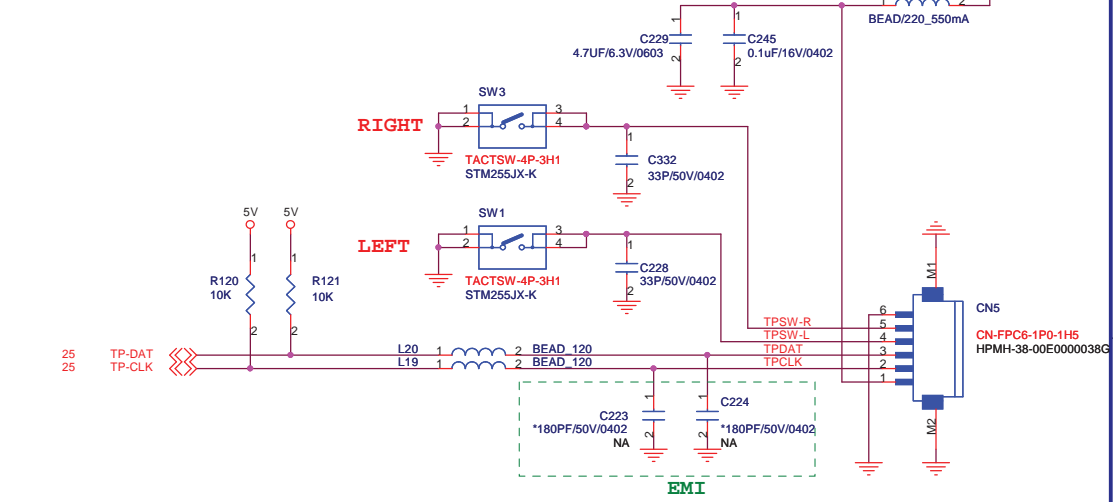
Project Name : ARWEN UA1		Title : USB / USB CON	
Size : C	Document Number : HPMH-40GAB4000-D000	Rev : D	
Date : Monday, August 17, 2009		Sheet : 22 of 35	



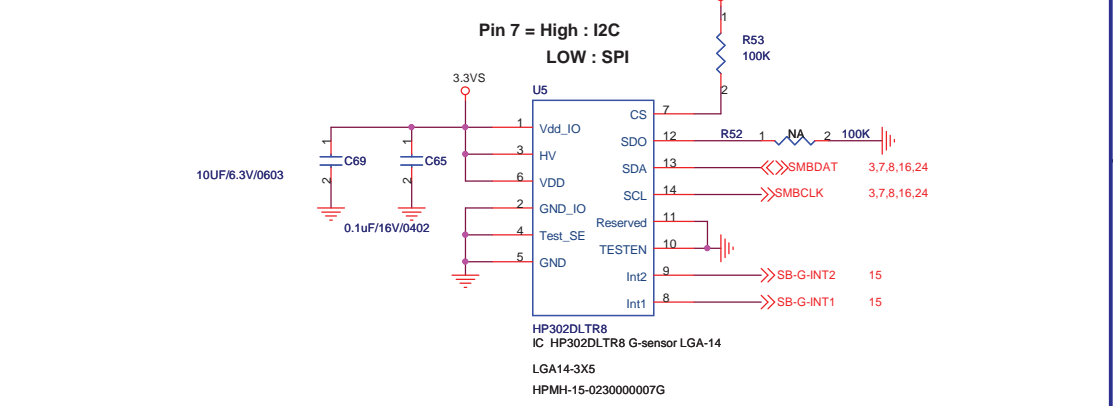
Blue Tooth



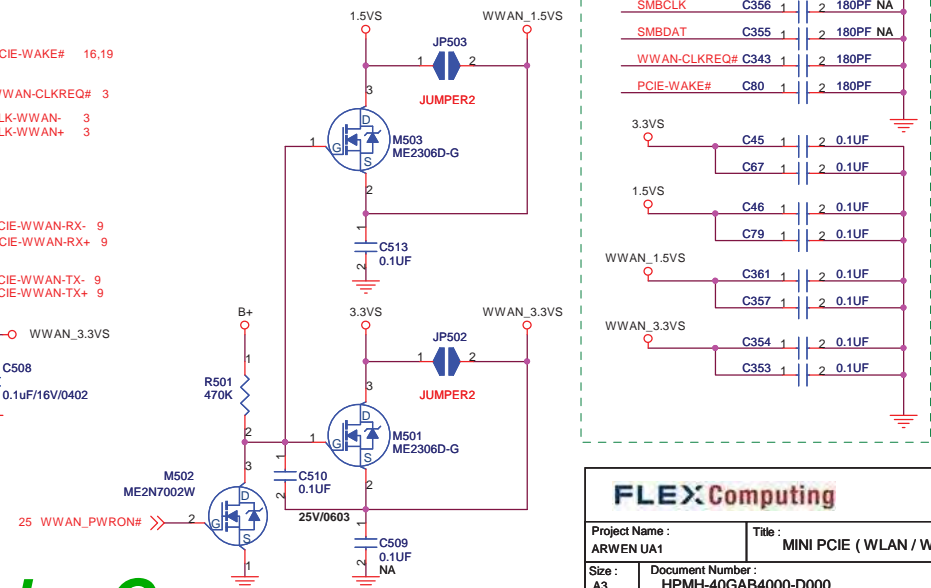
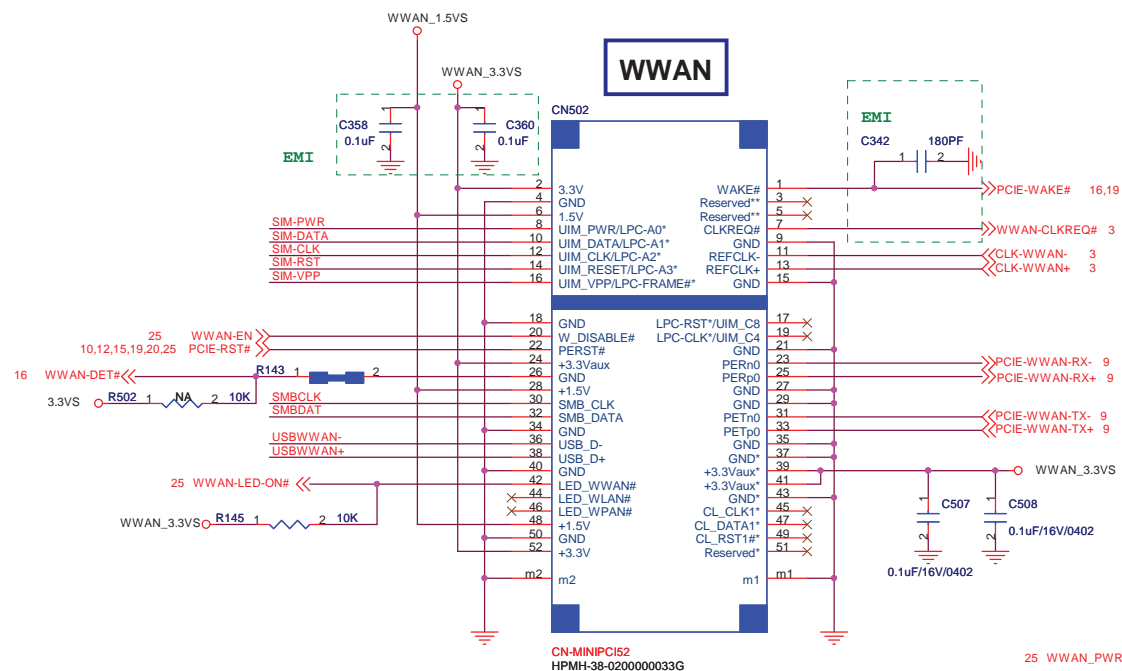
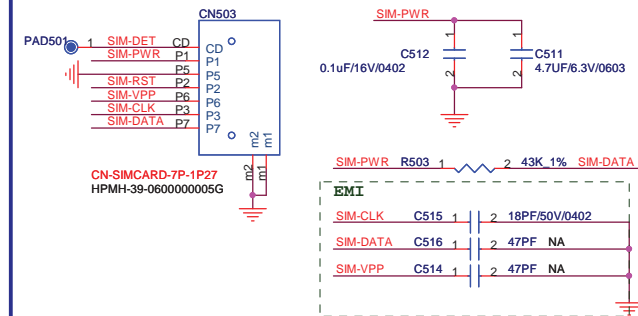
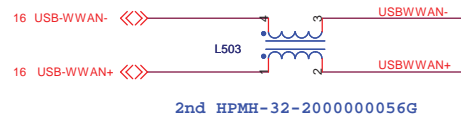
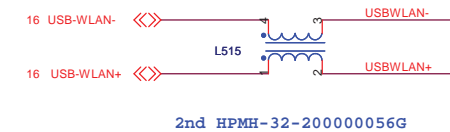
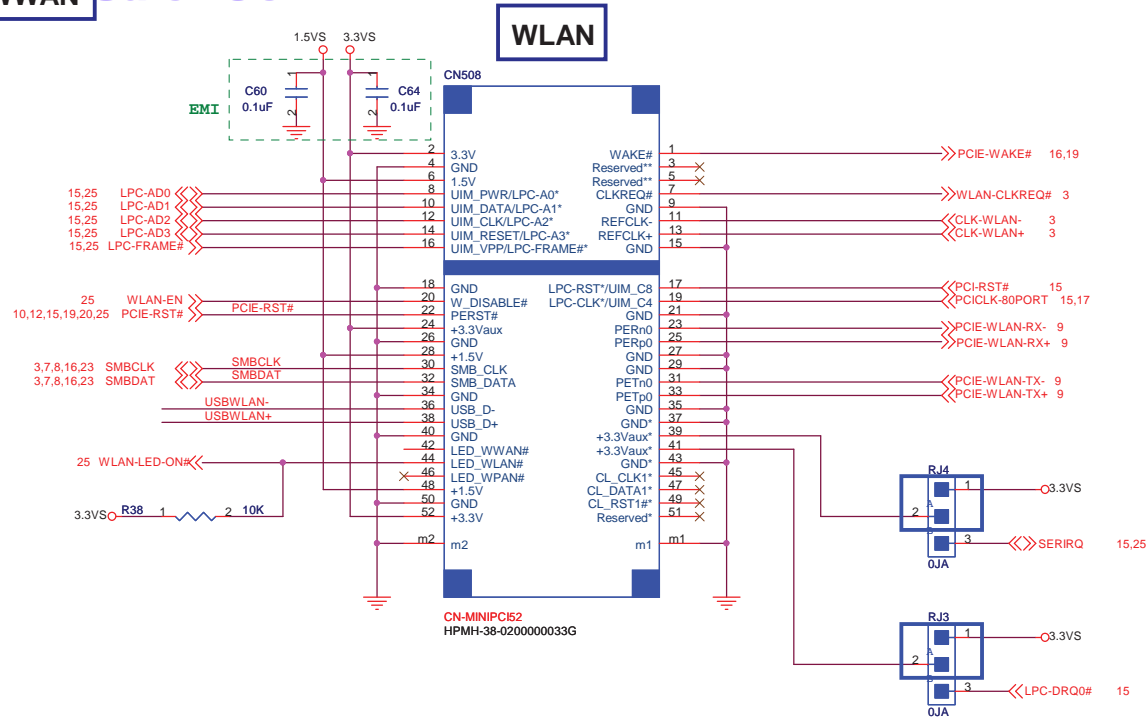
Touch Pad

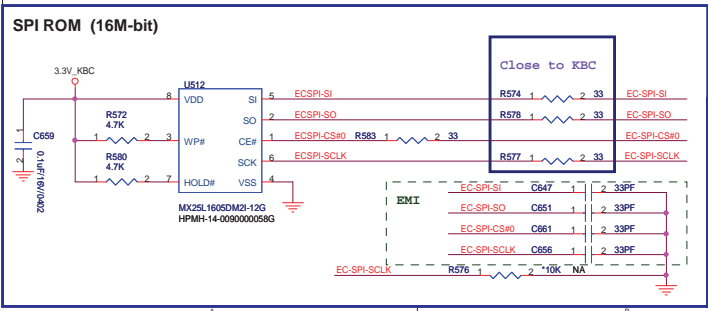
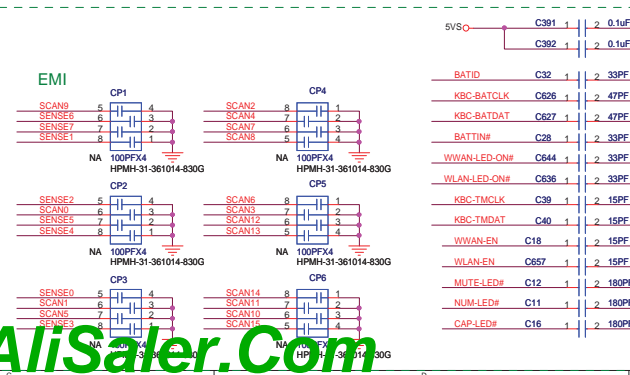
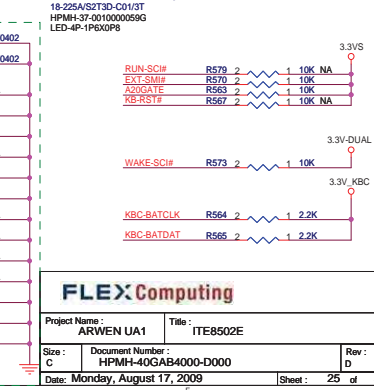
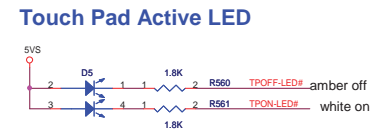
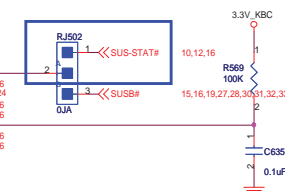
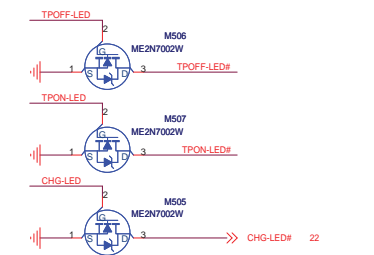
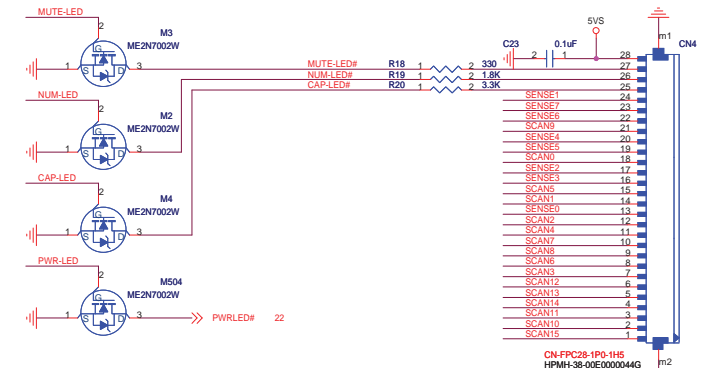
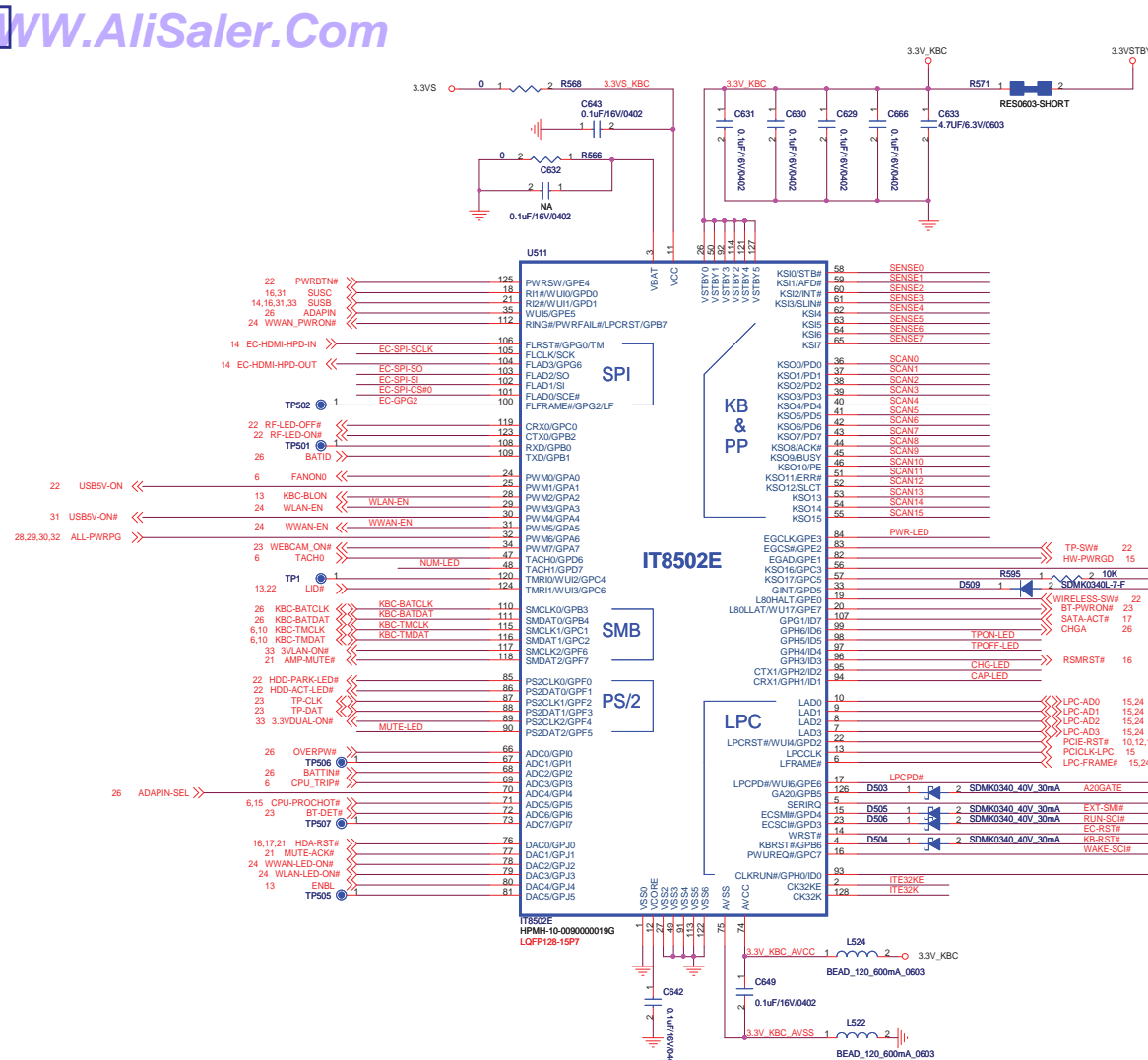


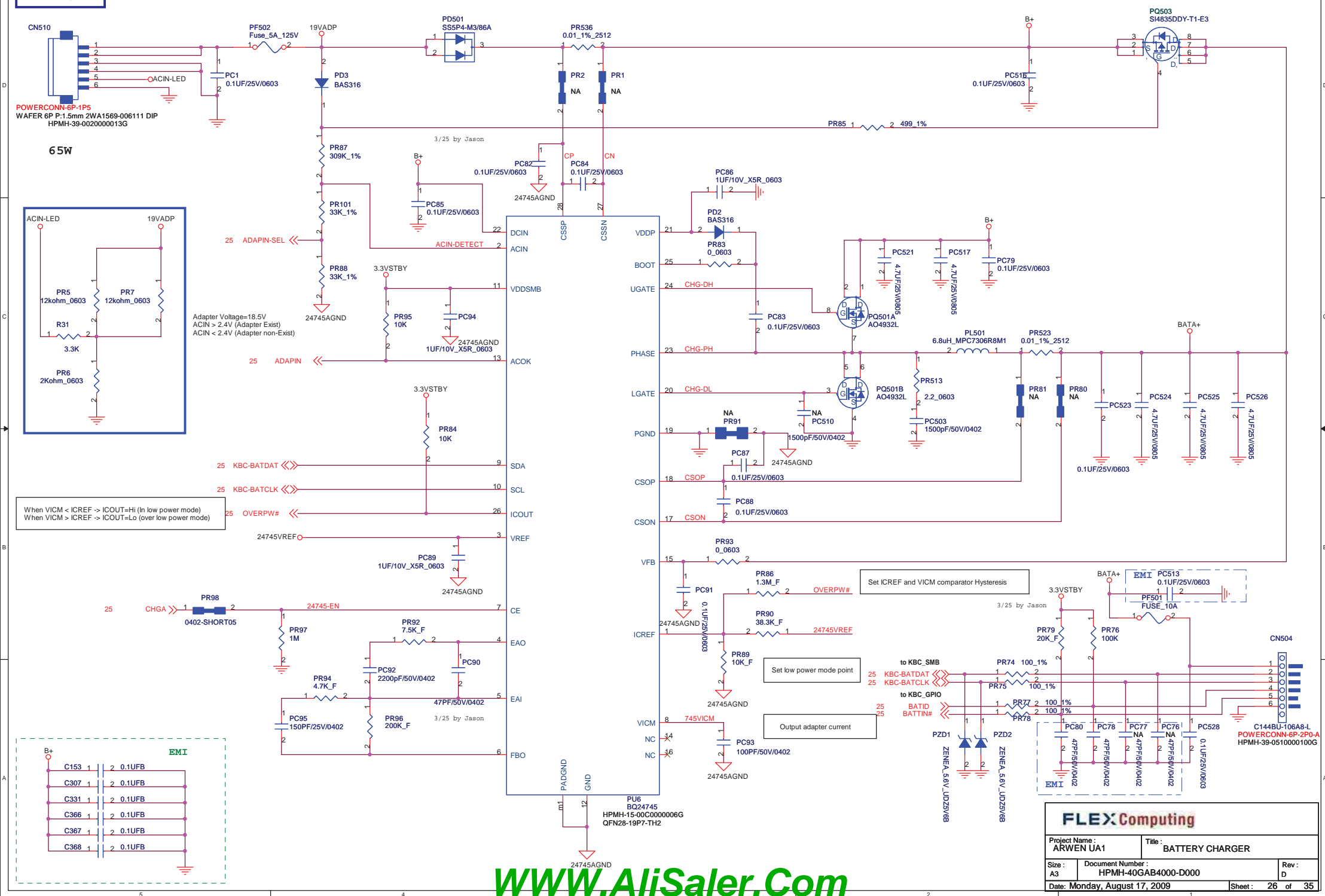
G-Sensor

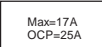







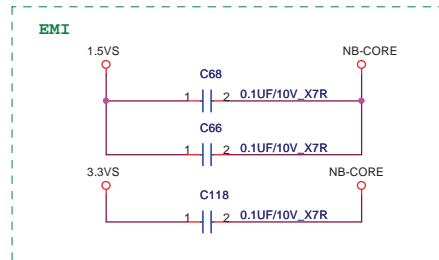
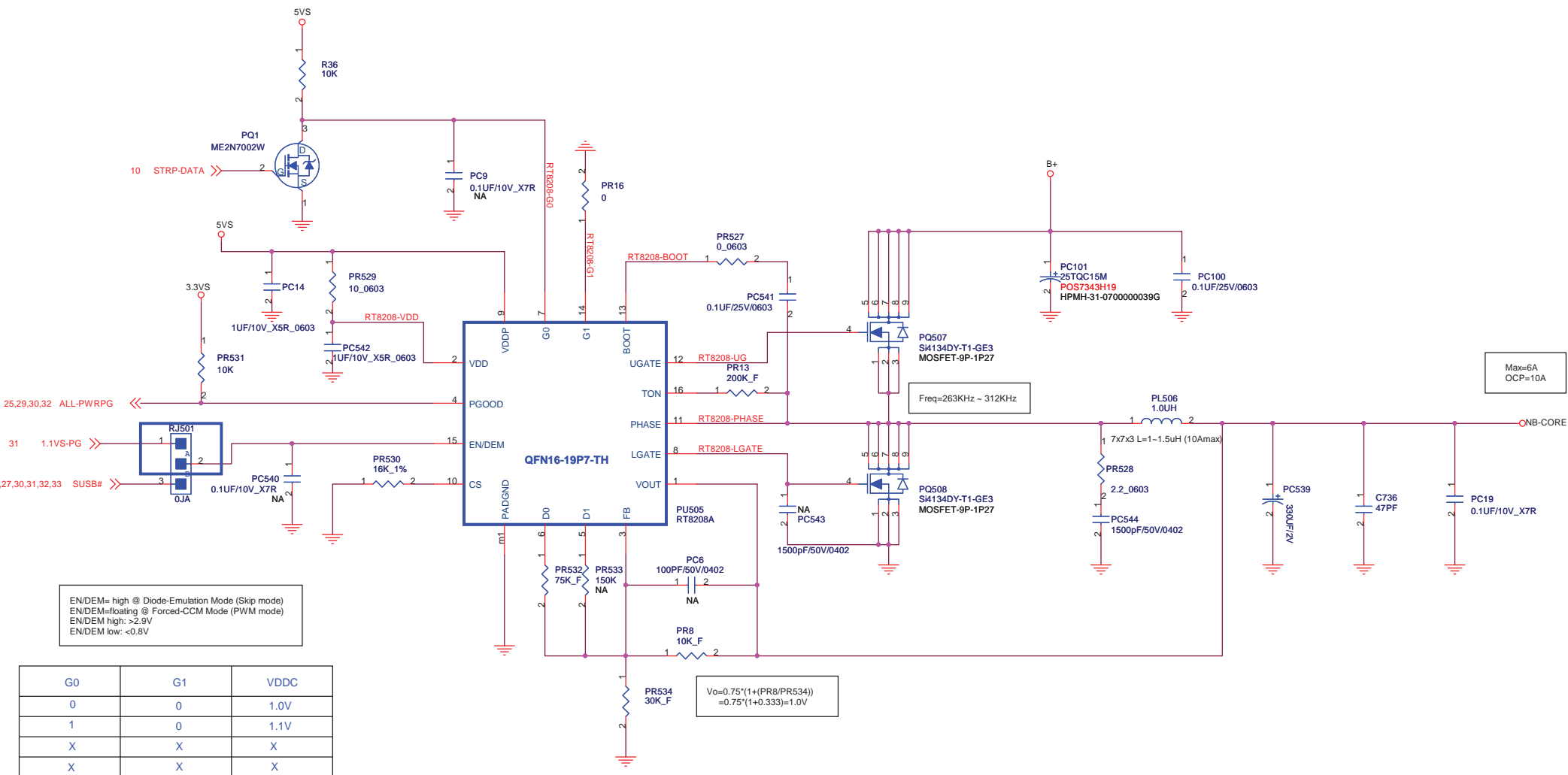




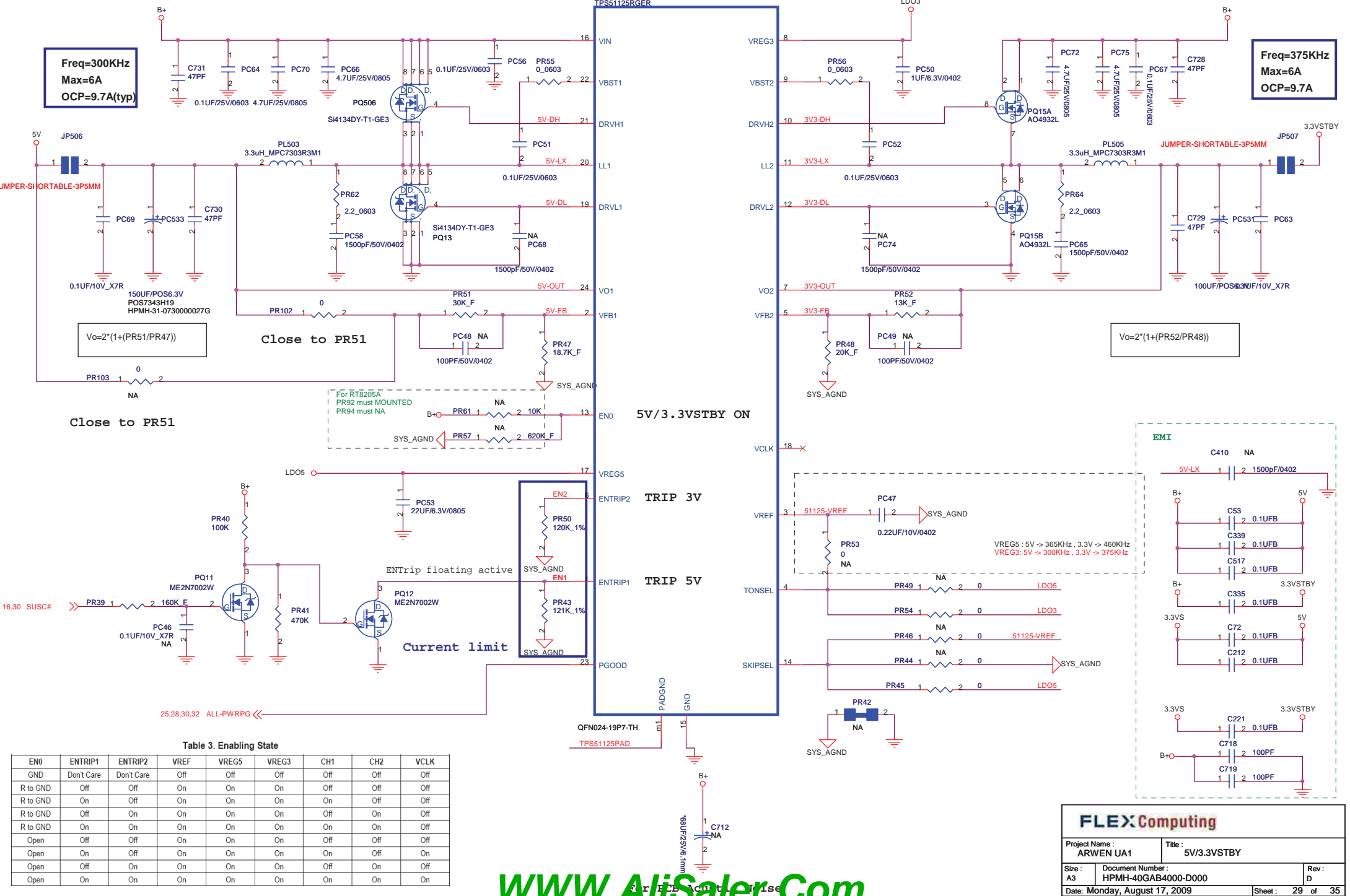


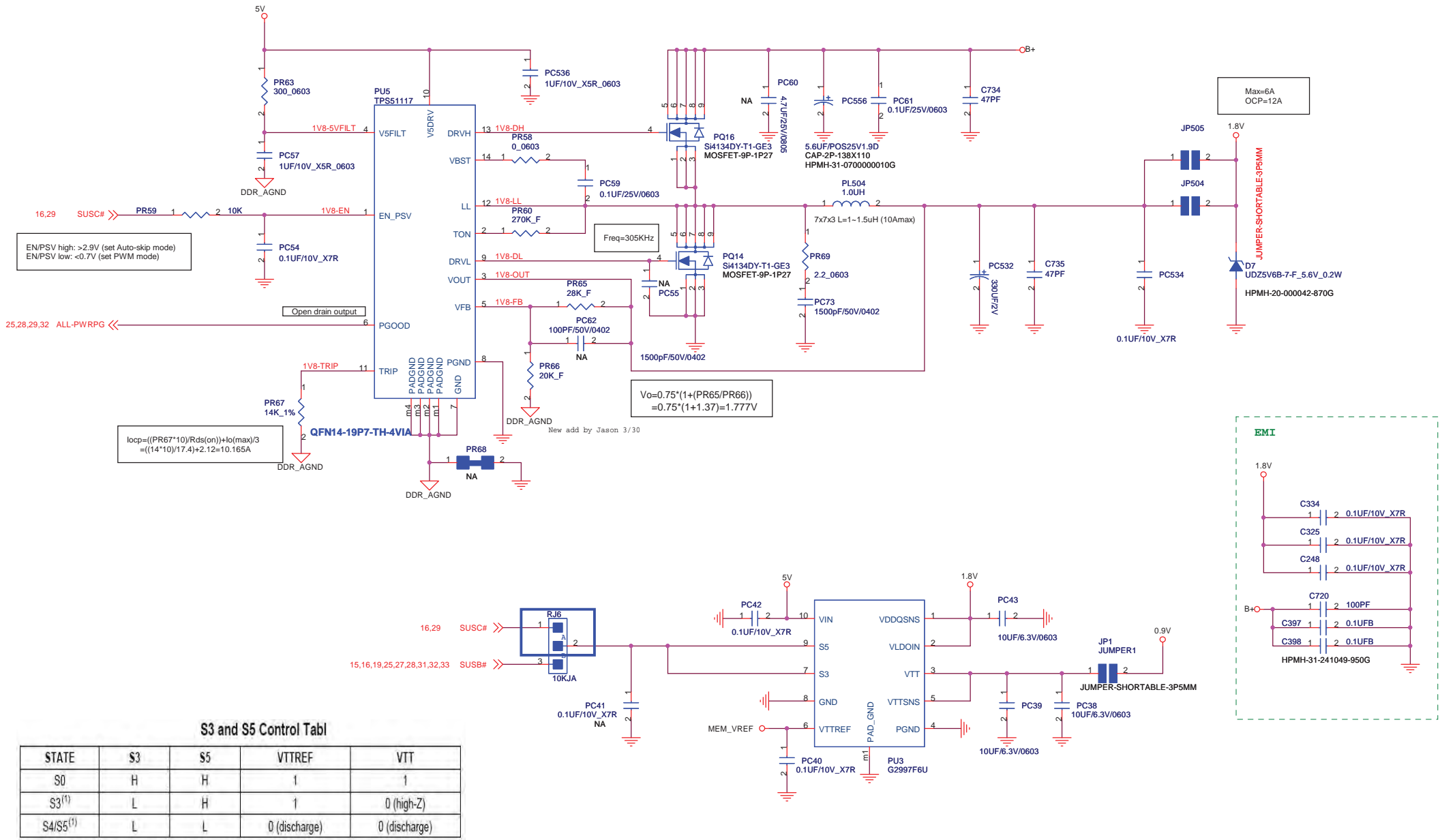
			
Project Name : ARWEN UA1		Title : CPU_CORE	
Size : A3	Document Number : HPMH-40GAB4000-D000		Rev : D
Date: Monday, August 17, 2009		Sheet: 27	of 35

NB\_CORE





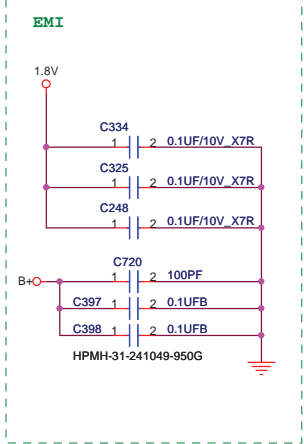
[illegible]

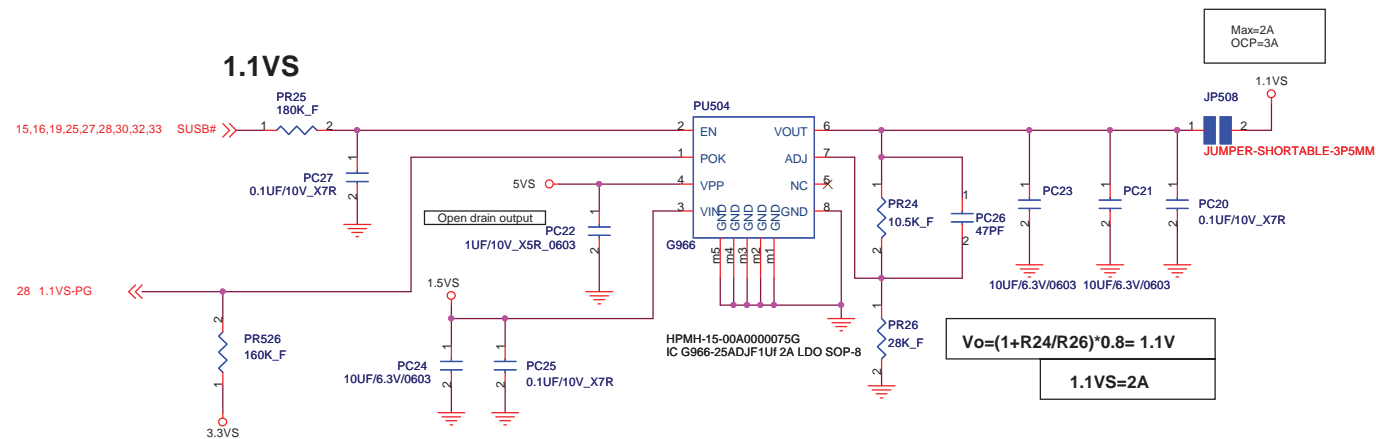


S3 and S5 Control Tabl

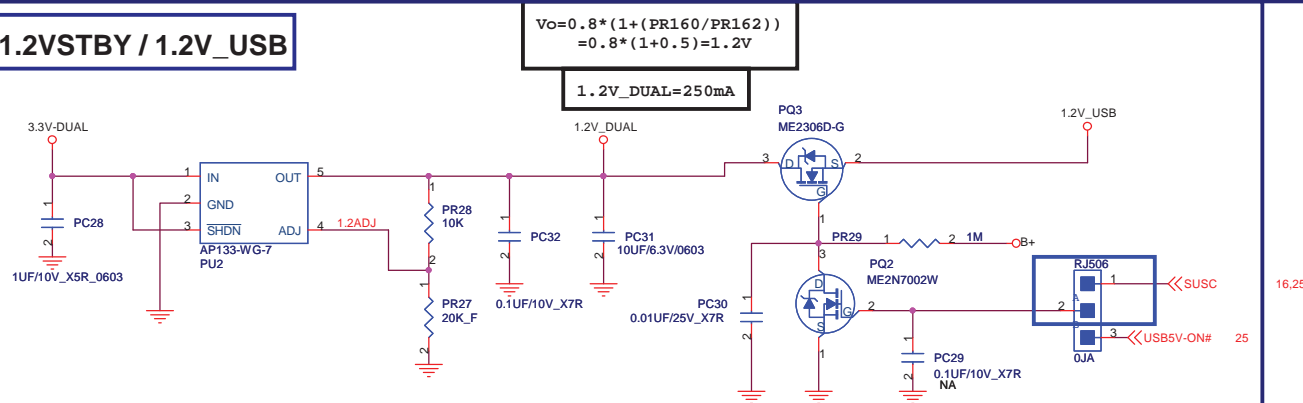
STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3 <sup>(1)</sup>	L	H	1	0 (high-Z)
S4/S5 <sup>(1)</sup>	L	L	0 (discharge)	0 (discharge)

(1) In case S3 is forced to H and S5 to L, VTTREF is discharged and VTT is at High-Z state. This condition is NOT recommended.

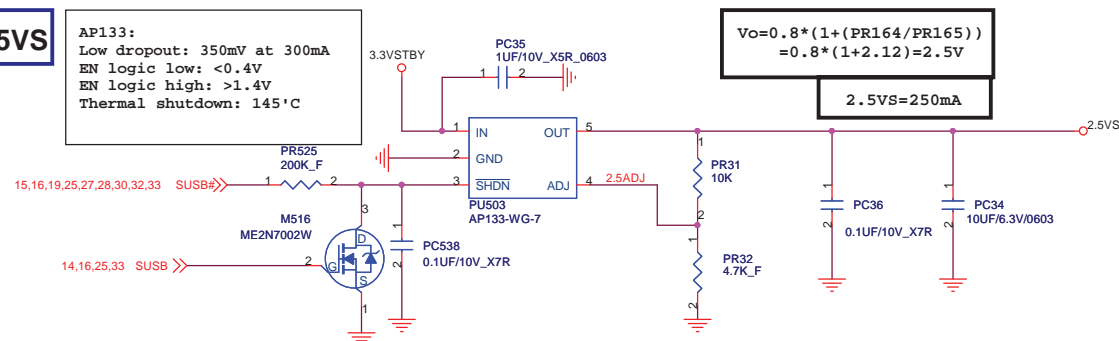


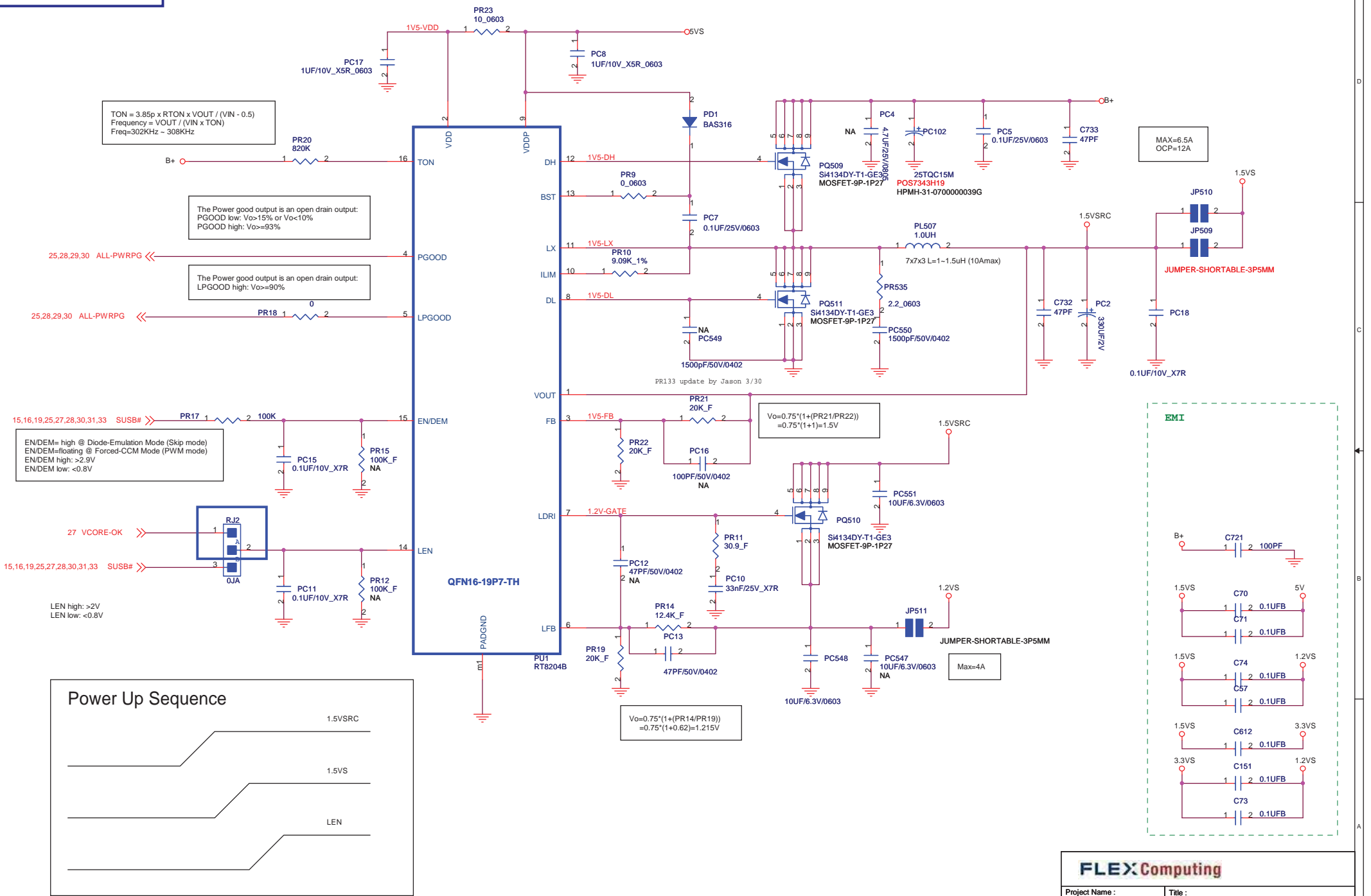


## 1.2VSTBY / 1.2V\_USB



## 2.5VS





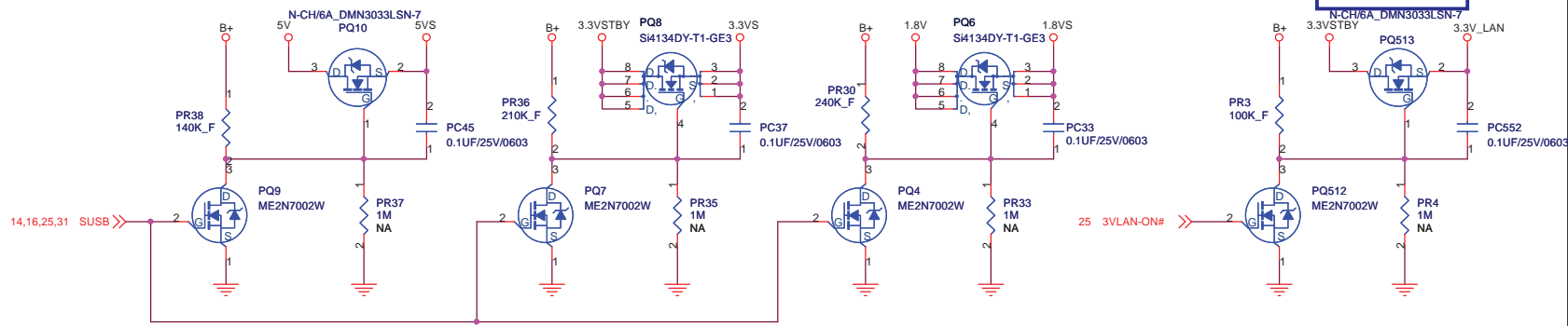
S4/S3 OFF

5VS

3.3VS

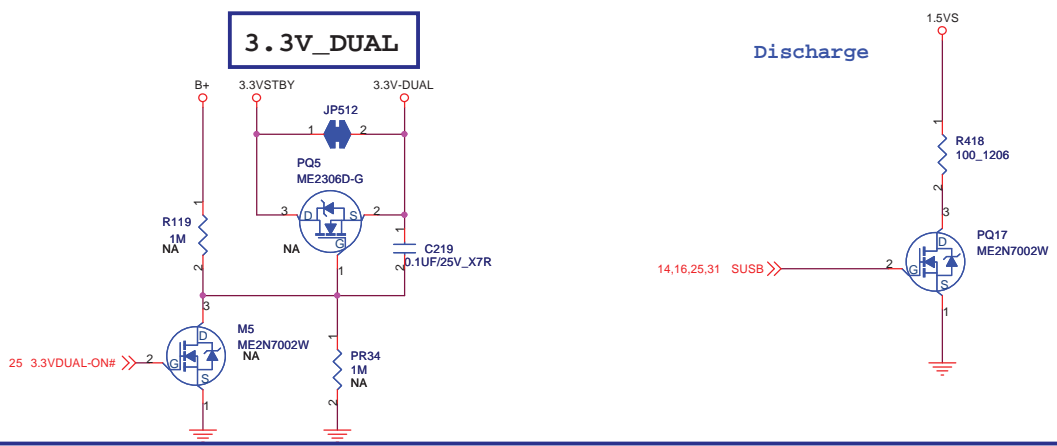
1.8VS

LAN\_3.3V



3.3V\_DUAL

Discharge

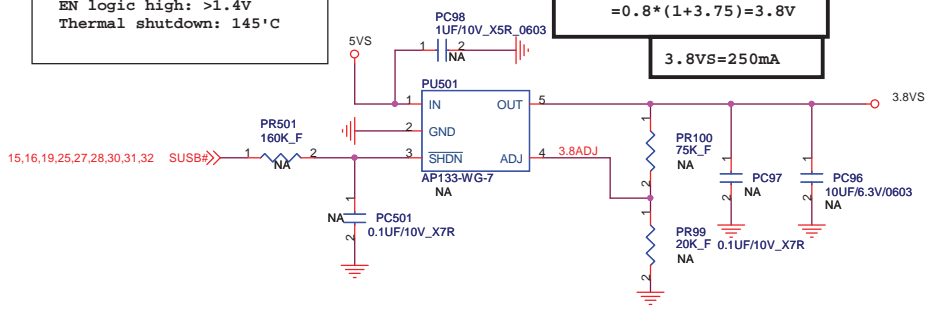


AP133:  
Low dropout: 350mV at 300mA  
EN logic low: <0.4V  
EN logic high: >1.4V  
Thermal shutdown: 145°C

3.8VS

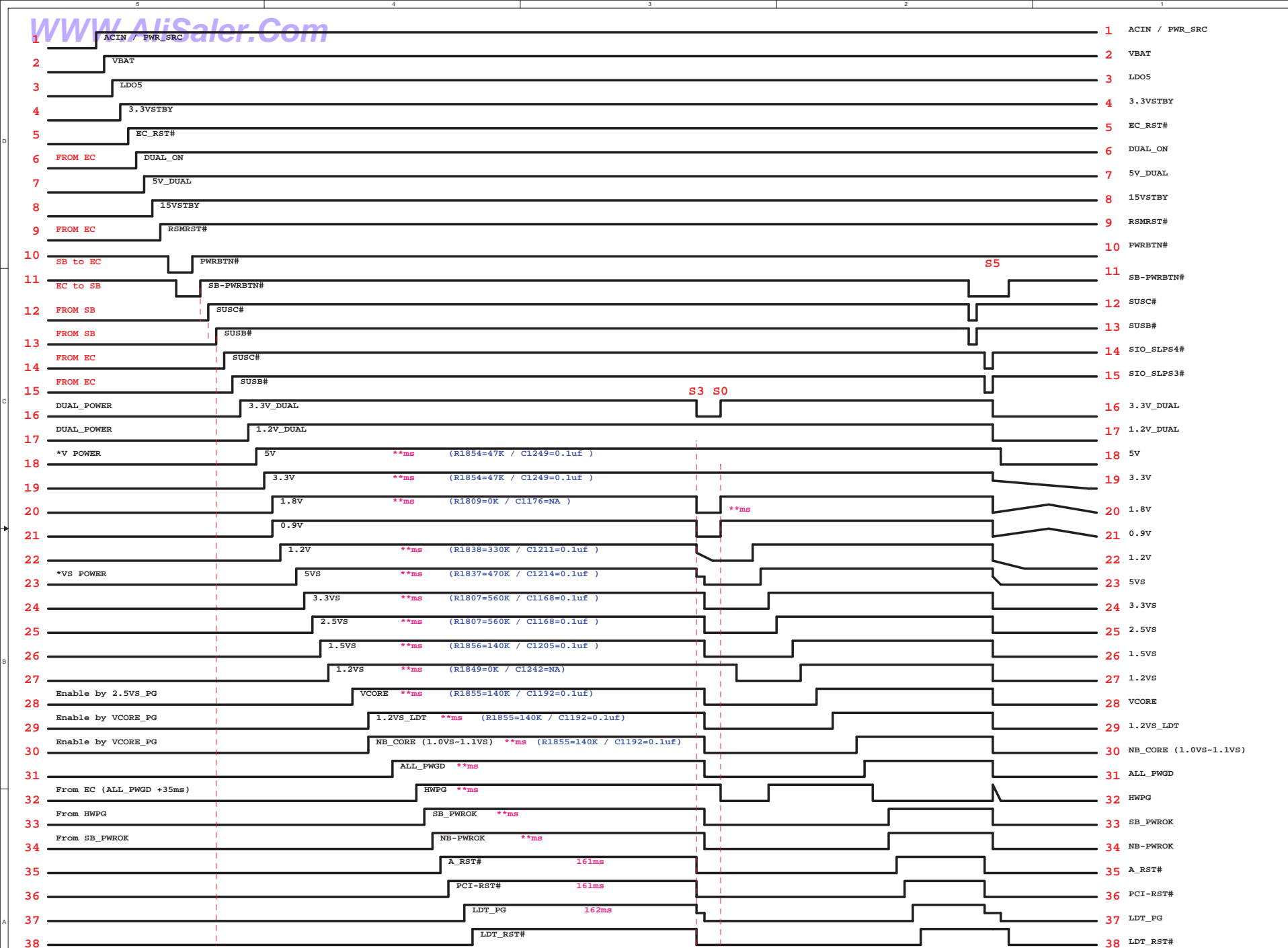
$$V_o = 0.8 * (1 + (PR100 / PR99)) = 0.8 * (1 + 3.75) = 3.8V$$

3.8VS=250mA



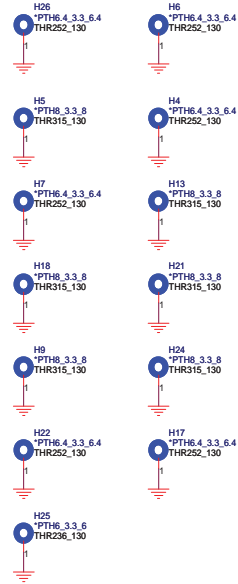
FLEX Computing

Project Name : ARWEN UA1		Title : VVS/VGA POWER	
Size : Custom	Document Number : HPMH-40GAB4000-D000		Rev : D
Date: Monday, August 17, 2009		Sheet : 33 of 35	





MB x 16



FID1 \*FIDUCIAL CAD-016  
 NC, NO CONNECT TO ANY.

FID3 \*FIDUCIAL CAD-016  
 NC, NO CONNECT TO ANY.

FID4 \*FIDUCIAL CAD-016  
 NC, NO CONNECT TO ANY.

FID5 \*FIDUCIAL CAD-016  
 NC, NO CONNECT TO ANY.

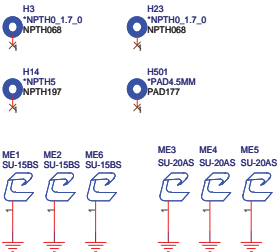
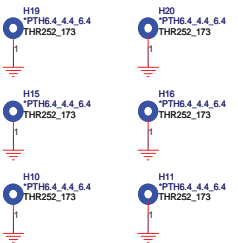
FID6 \*FIDUCIAL CAD-016  
 NC, NO CONNECT TO ANY.

FID7 \*FIDUCIAL CAD-016  
 NC, NO CONNECT TO ANY.

FID8 \*FIDUCIAL CAD-016  
 NC, NO CONNECT TO ANY.

FID2 \*FIDUCIAL CAD-016  
 NC, NO CONNECT TO ANY.

CPU/VGA x 8



EMI1  
 SPRING\_HEIGHT\_40  
 HPMH-B268511G00004  
 EMI-3L5X2W4H  
 2nd source HPMH-B268511G00001

EMI5  
 SPRING\_HEIGHT\_12  
 HPMH-B268511G00005  
 EMI-3L5X2W4H2  
 2nd source HPMH-B268511G00003

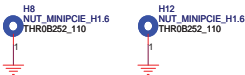
EMI2  
 SPRING\_HEIGHT\_25  
 HPMH-B268511G00006  
 EMI-2L6X1W5X2H5  
 2nd source HPMH-B268511G00002

EMI3  
 SPRING\_HEIGHT\_25  
 NA

EMI4  
 SPRING\_HEIGHT\_25

HPMH-B268511G00002  
 EMI-2L6X1W5X2H5

MINI CARD x 2



EMI x 2

